HIGH-VOLTAGE MIXED-SIGNAL IC

UC1638

160 x 240 4S STN LCD Controller-Driver

Preliminary Specifications
Datasheet Revision: 0.2

IC Version: c_A
November 22, 2012

ULTRACHIP

The Coolest LCD Driver, Ever!!

TABLE OF CONTENT

UC1638

Single-Chip, Ultra-Low Power
160COM x 240SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1638c is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and FRM (Frame Rate Modulation) gray-shade modulation scheme to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power COM and SEG drivers, UC1638c contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, battery operated hand held devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 160x240 matrix STN LCD with 4 gray shades and B/W Mode.
- A software-readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both page ordered and column ordered display buffer RAM access.
- Support industry standard 4-wire (S9), 3-wire (S8), and 2-wire (I^2C) serial interface and 8-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Consistent low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable frame rates, rainging from 36Hz to 66Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 5 temperature compensation coefficients.
- On-chip Software RESET command, make RST pin optional.
- Self-configuring 10x charge pump with on-chip pumping capacitors. Only 3/5 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S8, S9 or I2C) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range (Typ.) : 2.8V ~ 3.3V
  V_{DD} (analog) range (Typ.) : 2.8V ~ 3.3V
  LCD V_{OP} range: 6.3V ~ 17.5V
- MTP trimming available to support precise LCD contrast matching.
- Available in gold bump dies
  Bump pitch: 27 µM
  Bump gap: 12 µM
  Bump surface: 2,025 μM^2

ORDERING INFORMATION

Part Number	MTP	I^2C	Description
UC1638cGAA	Yes	Yes	Gold bumped die.

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT SENSITIVITY

The MTP memory cell is sensitive to photon excitation. Under extended exposure to strong ambient light, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light shields to realize full MTP content retention performance.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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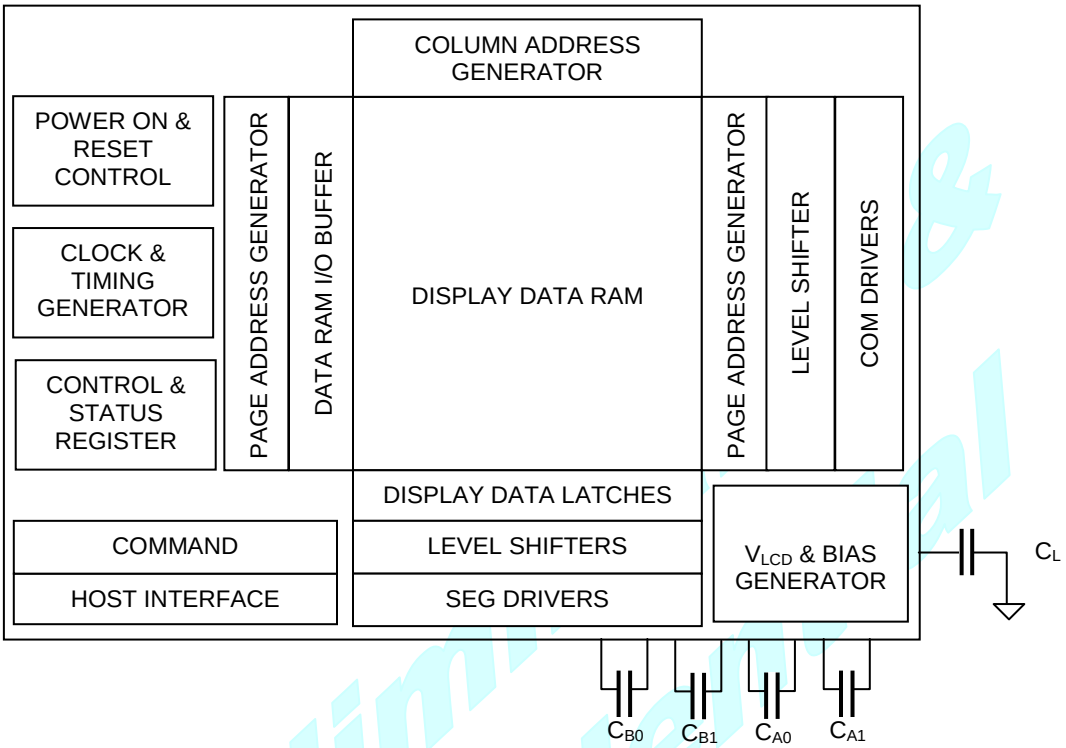
BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name (Pad Name)	Type	# of Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	14 14 5	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geq V_{DD2/3} \geq V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	17 14	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{A0+}, V_{A0-} V_{A1+}, V_{A1-} V_{B0+}, V_{B0-} V_{B1+}, V_{B1-}	PWR	3, 3 3, 3 3, 3 3, 3	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{AX} / C_{BX} of values between V_{AX+}~ V_{AX-} / V_{BX+}~V_{BX-}, respectively. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	4 5	High voltage LCD Power Supply. Capacitor C_L should be connected between V_{LCDOUT} and V_{SS}. When C_L is used, keep the trace resistance under 70Ω. When using internal pump, connect V_{LCDIN} and V_{LCDOUT} together. When using external pump, connect V_{LCDIN} to external power and keep V_{LCDOUT} floating.

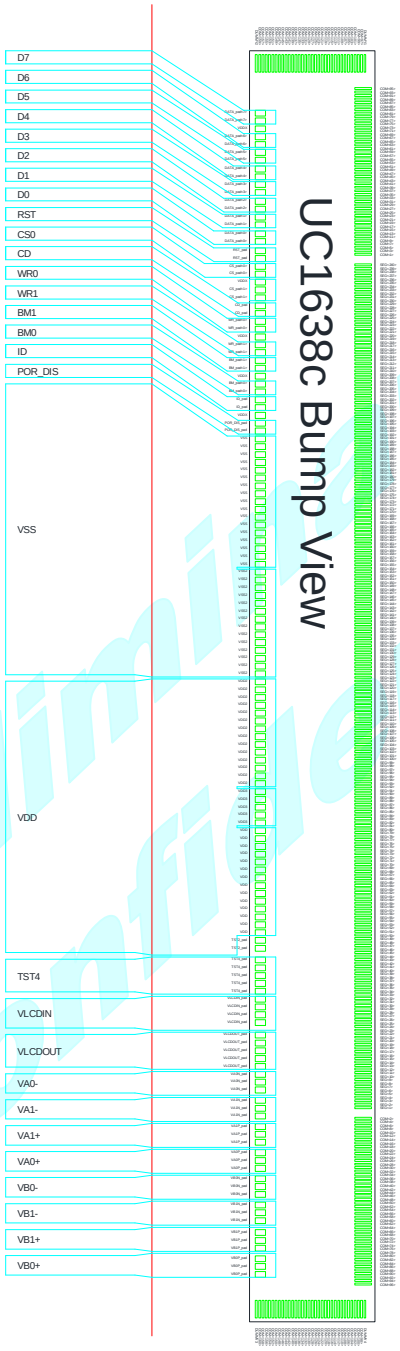
NOTE

- Recommended capacitor values:
  C_{AX}, C_{BX} : For panels of 3-inch or smaller, use 2.2uF capacitor;
  For panels bigger than 3 inches, use 5μF capacitor or higher.
  (Capacitor size depends on panel capacitance loading and actual image performance.)
  C_L : 330nF (25V) is appropriate for most applications.
- To avoid the correction of digital signals being affected by the charging/discharging of V_{AX} or V_{BX}, do not overlay C_{AX}, C_{BX} with the digital layout while FPC wiring.

<table>
<tr><th>Pin Name
(Pad Name)</th><th>Type</th><th># of Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1
(BM_pad<0>
BM_pad<1>)</td><td>I</td><td>2
2</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and DB[1]:
<table>
<tr><th>Mode</th><th>BM[1:0]</th><th>DB[1]</th></tr>
<tr><td>8080 (8-bit)</td><td>10</td><td>Data</td></tr>
<tr><td>6800 (8-bit)</td><td>11</td><td>Data</td></tr>
<tr><td>4-wire SPI w/ 8-bit token (S8)</td><td>00</td><td>0</td></tr>
<tr><td>3-wire SPI w/ 9-bit token (S9)</td><td>01</td><td>--</td></tr>
<tr><td>2-wire SPI (I^2C)</td><td>00</td><td>1</td></tr>
</table></td></tr>
<tr><td>CS0
CS1
(CS_pad<0>
CS_pad<1>)</td><td>I</td><td>2
2</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, DB[7:0] will be high impedance.</td></tr>
<tr><td>RST
(RST_pad)</td><td>I</td><td>2</td><td>When RST=”L”, IC is in RESET state and all control registers are re-initialized to their default states.
An RC Filter has been included on-chip. There is no need for external RC noise filter.</td></tr>
<tr><td>CD
(CD_pad)</td><td>I</td><td>2</td><td>Select Control data or Display data for read/write operation.
”L”: Control data ”H”: Display data
In S9 mode, this pin is not used. Connect it to Vss.</td></tr>
<tr><td>ID
(ID_pad)</td><td>I</td><td>2</td><td>ID pin is for production control.
The connection will affect the content of PID when using the <code>Get Status</code> command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1
(WR_pad<0>
WR_pad<1>)</td><td>I</td><td>2
2</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>DB7~DB0
(DATA_pad<7> ~
DATA_pad<0>)</td><td>I/O</td><td>2x8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect DB[0] to SCK, DB[3] to SDAI for write and DB[5:4] to SDAO for read.
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8-bit
(BM=1x)</td><td colspan="8">DB[7:0]</td></tr>
<tr><td>S8
(BM=00)</td><td>ACK</td><td>ACK</td><td>SDAO</td><td>SDAO</td><td>SDAI</td><td>–</td><td>0</td><td>SCK</td></tr>
<tr><td>S9
(BM=01)</td><td>ACK</td><td>ACK</td><td>SDAO</td><td>SDAO</td><td>SDAI</td><td>–</td><td>1</td><td>SCK</td></tr>
<tr><td>I^2C
(BM=00)</td><td>–</td><td>–</td><td>SDAO</td><td>SDAO</td><td>SDAI</td><td>–</td><td>1</td><td>SCK</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
</table>

Pin Name (Pad Name)	Type	# of Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG240 (SEG_pad<1> ~ SEG_pad<240>)	HV	240	SEG (column) driver outputs. Support up to 240 pixels. Leave unused drivers open-circuit.
COM1 ~ COM160 (COM_pad<1> ~ COM_pad<160>)	HV	160	COM (row) driver outputs. Support up to 160 rows. Leave unused COM drivers open-circuit.
Note: Several control registers will specify "0 based index" for COM and SEG electrodes. In those situations, COM*x* or SEG*x* will correspond to index *x*-1, and the value ranges for those index registers will be 0~159 for COM and 0~239 for SEG.			
MISC. PINS			
POR_DIS (POR_DIS_pad)	I	2	Power-ON reset control. Connect POR_dis to V_{DD} for "H"; to V_{SS} for "L". "L": Power-ON Reset Enabled "H": Power-ON Reset Disabled
TST2	I/O	2	Test I/O pin for UltraChip's use only. Leave it open during normal use.
TST4	I	5	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage programming power supply for MTP operation. For COG design with MTP options, please wire out TST4 with an ITO trace resistance 30 ~ 70 Ω.
Dummy	–	4	Dummy pins are NOT connected inside the IC.
Note: R_L: 3.3MΩ ~ 10MΩ to act as a draining circuit when V_{DD} is shut down abruptly.			

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The typical operation condition of UC1638c, V_{DD}=2.8V, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 20 Ω or lower; V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} drop to below 2.7V during high speed data-write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1638c contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1638c will be described in the next two sections: Command Table and Command Description.

Name: The Symbolic reference of the register.
Note that some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after System-Reset.

Name	# of Bits	Default	Description
SL	8	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and 159. Setting SL outside of this range causes undefined effect on the displayed image.
CR	9	000H	Returned Column Address. Useful for cursor implementation.
CA	9	000H	Column Address of Display Data RAM (Used in Host for Display Data RAM access. Value range: 0 ~ 239)
PA	6	00H	Page Address of Display Data RAM (Used in Host to access Display Data RAM. Value range: 0 ~ 39) When DC[4:3]=10b PA[5] : select Write Pattern 0 or 1 PA[4:0] : set SRAM page address When DC[4:3]=00b PA[5:0] : set SRAM page address
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 6 01b: 10 10b: 11 **11b: 12**
TC	3	4H	Temperature Compensation (per ^{o}C) 000b: -0.00% **100b: -0.05%** 101b: -0.10% 110b: -0.15% 111b: -0.20%
PM	8	54H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PC	1	1H	Power Control. 0b: External V_{LCD} **1b: Internal V_{LCD}** (10x charge pump)
DC	6	08H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray Shade and B/W mode 0b: B/W Mode **1b: 4-Shade Mode** DC[4]: Input type for On/Off mode **0b: 2 bits per pixel** 1b: 1 bit per pixel DC[5]: Display pattern selection **0b: Pattern 0** 1b: Pattern 1 (Enabled only when On/Off mode and DC[4]=1)
AC	5	01H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0 : Column (CA) first** 1 : Row (PA) first AC[2]: RID: PA (Page Address) auto increment direction (**0 : +1** 1 : -1) AC[3]: Window Program Enable **0 : Disable** 1 : Enable AC[4]: CUM – Cursor Update Mode. (Default **0:OFF**) When CUM=1, CA increase on Write only

Name	# of Bits	Default	Description
LC	9	098H	LCD Control: LC[0]: MX, Mirror X. SEG/Page_C sequence inversion (Default: **OFF**) LC[1]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[3:2]: Line Rate (= Frame-Rate * Mux-Rate) 00b: 17.5 Klps 01b: 21.3 Klps **10b: 26.0 Klps** 11b: 31.7 Klps Line Rate (for On/Off mode): 00b: 8.6 Klps 01b: 10.5 Klps **10b: 12.8 Klps** 11b: 15.6 Klps (Klps: Kilo-line-per-second) LC[8:5]: Gray-Shade control. LC[7:6] / Gray-shade Level 2: 00→3, 01→4, **10→5**, 11→6 LC[5:4] / Gray-shade Level 1: 00→1, **01→2**, 10→3, 11→4 LC[8]: Partial Display Control **0b: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1
NIV	8	00H	N-line Inversion: NIV[6:0]: **0000000b: Disable Inversion Function** 0000001b~1010000b: Invert every 2~80 lines NIV[7]: 0b: **no-XOR** 1b: XOR
CSF	1	0H	COM Scan Function **0: Interlace Scan** 1: Progressive Scan
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN >= DEN >= DST+ 9
WPC0	8	00H	Window program starting column address. Value range: **0** ~239.
WPP0	6	00H	Window program starting Page Address. Value range: **0**~39. When DC[4:3]=10b, Value range: 0~19
WPC1	8	EFH	Window program ending column address. Value range: 0~**239**.
WPP1	6	27H	Window program ending Page Address. Value range: 0~**39**. When DC[4:3]=10b, Value range: 0~19. (Default : 13H)
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000 : Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip use only. MTPC[3] : MTP Enable (auto clear after MTP command action done) MTPC[4] : Use/Ignore MTP value. 0: Ignore **1: Use**
MTPM	6	00H	MTP Write Mask. Bit = 1: program, **Bit = 0: no action**.
RV	8	00H	MTP Read PM (Vlcd = 6.3V with BR = 00b)
WV	8	16H	MTP Program/ Erase PM (Vlcd = 13V with BR = 10b)
RT	8	04H	MTP Read Timer (35mS when default Frame Rate)
WT	8	60H	MTP Program/ Erase Timer (200mS when default Frame Rate)

Name	# of Bits	Default	Description
APC0~3 [7:0]	8x4	N/A	Advanced Product Configuration. For UltraChip only. Do *NOT* use.
Status Register			
POR	1	PIN	Access the connected status of POR_dis pin. 1/0 : disable/enable POR
MX, MY	1, 1		MX : Mirror X, that is LC[1]. MY : Mirror Y, that is LC[2].
PID	1	PIN	Access the connected status of ID pin.
DE	1		DE : display enabled.
WS	1	-	MTP Operation Succeeded
MD	1	-	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	-	MTP programming in-progress
Ver	2		Ver : IC version. Default : 00b
PMO	6	00H	PM offset. PMO[5]=1: The effective PM value, PMV = PM – PMO[4:0] PMO[5]=0: The effective PM value, PMV = PM + PMO[4:0]

COMMAND SUMMARY

The following is a list of host commands supported by UC1638c:

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte (double-byte command)	0	0	0	0	0	0	0	0	0	1	Write 1 byte	N/A
		1	0	#	#	#	#	#	#	#	#		
2.	Read Data Byte (double-byte command)	0	0	0	0	0	0	0	0	1	0	Read 1 byte	N/A
		1	1	#	#	#	#	#	#	#	#		
3.	Get Status (triple-byte command)	0	0	0	0	0	0	0	0	1	1	Get Status	N/A
		1	1	POR	MX	MY	PID	DE	WS	MD	MS		
		1	1	Ver[1:0]		PMO[5:0]							
4.	Set Column Address (double-byte command)	0	0	0	0	0	0	0	1	0	0	Set CA[7:0]	00H
		1	0	#	#	#	#	#	#	#	#		
5.	Set Temp. Compensation	0	0	0	0	1	0	0	#	#	#	Set TC[2:0]	100b
6.	Set Pump Control	0	0	0	0	1	0	1	1	0	#	Set PC[0]	1b
7.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	R	R	R	R = 0~3, Set APC[R][7:0]	N/A
		1	0	#	#	#	#	#	#	#	#		
8.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0H
9.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0H
	Set Page Address MSB	0	0	0	1	1	1	0	0	#	#	Set PA[5:4]	0H
10.	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	54H
		1	0	#	#	#	#	#	#	#	#		
11.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0: Disable
12.	Set COM Scan Function	0	0	1	0	0	0	0	1	1	#	Set CSF[0]	0b
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Display mode	0	0	1	0	0	1	0	1	#	#	Set DC[5:4]	00b
15.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[3:2]	10b
16.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[1:0]	00b
19.	Set N-Line Inversion (double-byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[7:0]	00H
		1	0	#	#	#	#	#	#	#	#		
20.	Set Display Enable (double-byte command)	0	0	1	1	0	0	1	0	0	1	Set DC[3:2]	10b
		1	0	1	0	1	0	1	1	#	#		
21.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[5:4]	01b
22.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
23.	System Reset (double-byte command)	0	0	1	1	1	0	0	0	0	1	System Reset	N/A
		1	0	1	1	1	0	0	0	1	0		
24.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		1	0	#	#	#	#	#	#	#	#		
26.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[4]=0, CA=CR	N/A
28.	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[4]=1, CR=CA	N/A
29.	Set COM End (double-byte command)	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]	159
		1	0	#	#	#	#	#	#	#	#		
30.	Set Partial Display Start (double-byte command)	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]	0
		1	0	#	#	#	#	#	#	#	#		
31.	Set Partial Display End (double-byte command)	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	159
		1	0	#	#	#	#	#	#	#	#		

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
32.	Set Window Programming Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0[7:0]	0
		1	0	#	#	#	#	#	#	#	#		
33.	Set Window Programming Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0[5:0]	0
		1	0	0	0	#	#	#	#	#	#		
34.	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1[7:0]	239
		1	0	#	#	#	#	#	#	#	#		
35.	Set Window Programming Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1[5:0]	39
		1	0	0	0	#	#	#	#	#	#		
36.	Enable Window Program	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Disable
37.	Set MTP Operation control (double-byte command)	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H
		1	0	0	0	0	#	#	#	#	#		
38.	Set MTP Write Mask (double-byte command)	0	0	1	0	1	1	1	0	0	1	Set MTPM[5:0]	00H
		1	0	0	0	#	#	#	#	#	#		
39.	Set MTP Read Potentiometer	0	0	1	1	1	1	1	0	1	0	Set RV[7:0] (BR=00b)	00H
		1	0	#	#	#	#	#	#	#	#		
40.	Set MTP Program/Erase Potentiometer	0	0	1	1	1	1	1	0	1	1	Set WV[7:0] (BR=10b)	16H
		1	0	#	#	#	#	#	#	#	#		
41.	Set MTP Write Timer (double-byte command)	0	0	1	1	1	1	1	1	0	0	Set WT[7:0]	60H
		1	0	#	#	#	#	#	#	#	#		
42.	Set MTP Read Timer (double-byte command)	0	0	1	1	1	1	1	1	0	1	Set RT[7:0]	04H
		1	0	#	#	#	#	#	#	#	#		

Warning: Any bit patterns other than the commands listed above may result in undefined behavior.

Notes:

(1) Any bit patterns other than the commands listed above may result in undefined behavior.

(2) The interpretation of commands (37)~(42) depends on register MTPC[3].

(3) After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always
a) Remove TST4 power source,
b) Do a full VDD ON-OFF-ON cycle.

COMMAND DESCRIPTION

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data (double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	8-bit data write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data (double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	1	1	8-bit data from SRAM							

Write/Read Data Byte (command 1, 2) operation uses internal Page Address register (PA) and Column Address register (CA). Four rows of LCD pixel image are defined as one row in SRAM. Each column of pixel corresponds to one column of SRAM data. PA and CA registers can be programmed by issuing `Set Page Address` and `Set Column Address` commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of PA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and PA will be increased or decreased, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 39), PA will be wrapped around to the other end of RAM and continue.

For 8-bit-bit interface, the first cycle of read is a dummy read. Please ignore the data read out.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status (triple-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	1	1	POR	MX	MY	PID	DE	WS	MD	MS
	1	1	Ver[1:0]		PMO[5:0]					

Status 1 definitions:
- POR: Power-On-Reset status of accessing to POR_DIS pin. (0: POR enabled, 1: POR disabled)
- MX: Status of register LC[0], mirror X.
- MY: Status of register LC[1], mirror Y.
- PID: Provide connection status of accessing to ID pin.
- DE: Display enable flag. DE=1 when display is enabled
- WS: MTP Command Succeeded
- MD: MTP Option (1 : MTP version, 0 : non-MTP version)
- MS: MTP action status

Status 2 definitions:
- Ver[1:0]: IC Version Code, 00 ~ 11. Default: 00
- PMO[5:0]: PM offset value.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address CA[7:0] (double-byte command)	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
	1	0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

Set SRAM column address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~239 (Default: 0)

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	TC2	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

TC[2:0]	Temperature Compensation
000b	-0.00% per ^{o}C
100b (Default)	**-0.05% per ^{o}C**
101b	-0.10% per ^{o}C
110b	-0.15% per ^{o}C
111b	-0.20% per ^{o}C

(6) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	**0**	PC0

Set PC[0] to program the build-in charge pump stages.

PC[0]	Pump Control
0b	External V_{LCD}
1b (Default)	**Internal V_{LCD} (10x charge pump)**

When using external pump, setting BR and setting PM are still necessary.

(7) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0] (double-byte command)	0	0	**0**	**0**	**1**	**1**	**0**	R	R	R
	1	0	APC[R][7:0] register parameter							

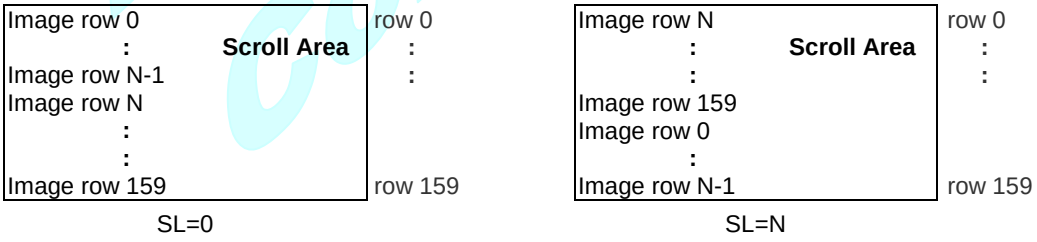
For UltraChip's use only. Please do NOT use.

(8) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	**0**	**1**	**0**	**1**	SL7	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 159.



(9) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA [3:0]	0	0	**0**	**1**	**1**	**0**	PA3	PA2	PA1	PA0
Set Page Address PA [5:4]	0	0	**0**	**1**	**1**	**1**	**0**	**0**	PA5	PA4

Set SRAM Page Address for read/write access. Possible value = **0**~39. UC1638c can store 2 B/W mode pictures in SRAM. Set PA[5] to specify which one to store. (Also refer to command "Set Display Mode".)

When DC[4:3]=10b
PA[5] : Write Pattern (0 or 1) selection
PA[4:0] : set SRAM page address

When DC[4:3] not = 00b
PA[5:0] : set SRAM page address

(10) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	1	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255** (Default: 54H, i.e. 84)

(11) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [8]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC8

This command is used to enable partial display function.

LC[8]	Partial Display function	Mux-Rate
0b (Default)	**Disable**	= CEN+1 (DST, DEN not used.)
1b	Enable	= DEN-DST+1

(12) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[0]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**1**	CSF0

CSF[0]	COM scan function
0b (Default)	**Interlace scan**
1b	Progressive Scan

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increase by one.

AC[1]: Auto-Increment order
0 : column (CA) increase (+1) first until CA reaches CA boundary, then PA will increase by (+/-1).
1 : page (PA) increase (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2]: RID, Page Address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether Page Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and PA. When Window Program is enabled (AC[3]=ON), see Command Description (32) ~ (35) for more details. When Window Program is disabled (AC[3]=OFF), the behavior of CA, PA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[3]=ON.

(14) SET DISPLAY MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Mode DC [5:4]	0	0	**1**	**0**	**0**	**1**	**0**	**1**	DC5	DC4

This command is enabled only when on/off mode. UC1638c can store 2 B/W mode pictures in SRAM. Set DC[5] to specify which one to display. (Also refer to command “Set Page Address”.)

DC[4]: Input type for On/off mode
0b: 2 bits per pixel 1b: 1 bit per pixel
DC[5]: Display Pattern selection (enabled only when DC[4]=1)
0b: Pattern 0 1b: Pattern 1

(15) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [3:2]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC3	LC2

Program LC [3:2] for line rate setting (Line-Rate = Frame-Rate x Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 108, 80, 56, and 40.

LC [4:3]	Line rate	
	when Mux Rate = 109~160	On/Off mode
00b	17.5 Klps	8.6 Klps
01b	21.3 Klps	10.5 Klps
10b (Default)	**26.0 Klps**	**12.8 Klps**
11b	31.7 Klps	15.6 Klps

(Klps: Kilo-Line-per-second)

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM. **(Default 0: OFF)**

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM. **(Default 0: OFF)**

(18) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [1:0]	0	0	**1**	**1**	**0**	**0**	**0**	LC1/MY	LC0/MX	**0**

This command is used for programming LC[1:0] for COM (page) mirror (MY), SEG (column) mirror (MX).

LC1 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC0 controls Mirror X (MX): MX is implemented by selecting the CA or 39-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

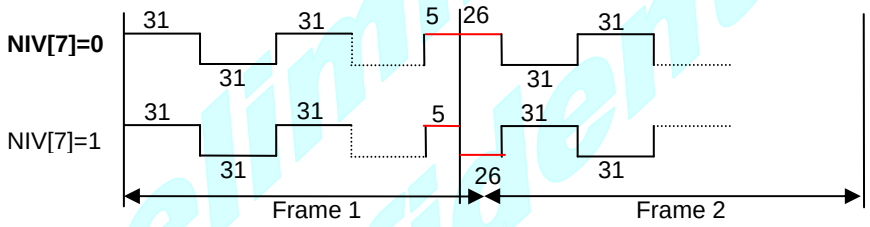
(19) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-Line Inversion NIV [7:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(double-byte command)	1	0	NIV7	NIV6	NIV5	NIV4	NIV3	NIV2	NIV1	NIV0

This command is used for programming NIV[7:0] for N-Line Inversion.

NIV[7]	Exclusive
0b (Default)	**no-XOR**
1b	XOR

NIV [6:0]	Inversion
000 0000b	**Disable Inversion Function**
000 0001b	Invert every 2 lines
:	:
101 0000b	Invert every 80 lines



(20) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [3:2]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1**
(double-byte command)	1	0	**1**	**0**	**1**	**0**	**1**	**1**	DC3	DC2

The command is for programming register DC[3:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit, and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1638c will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode. (Default **0: OFF**)

DC[3]: Gray Shade and B/W mode
0b: B/W Mode **1b: 4-Shade Mode**

For B/W mode, use data format for 4-shade-mode and UC1638c will convert them for B/W mode automatically.

Note : When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1638c for 5~10mS after setting DC[2] to 1 (Display ON).

(21) SET LCD GRAY SHADE 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[5:4]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	LC5	LC4

This command sets gray scale register LC[5:4] to control the voltage RMS separation between gray shade levels “01” and “10”.

LC[5:4]	Gray-shade Level	Gray-shade Intensity Mapped
00b	1	9 (full range: 0~36)
01b (Default)	**2**	**12** (full range: 0~36)
10b	3	15 (full range: 0~36)
11b	4	21 (full range: 0~36)

(22) SET LCD GRAY SHADE 2

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[7:6]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC7	LC6

This command sets gray scale register (LC[7:6]) to control the voltage RMS separation between gray shade levels “01” and “10”.

LC[7:6]	Gray-shade Level	Gray-shade Intensity Mapped
00b	3	15 (full range: 0~36)
01b	4	21 (full range: 0~36)
10b (Default)	**5**	**24 (full range: 0~36)**
11b	6	27 (full range: 0~36)

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset (double-byte command)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
	1	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (double-byte command)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
	1	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b = 6 01b = 10 10b = 11 **11b = 12**

(27) RESET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Return the cursor. AC[4]=0, CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset cursor update mode function. It will clear cursor update mode flag (AC[4]=0), and CA will be restored to its previous value, which was stored in CR (via Set Cursor Update Mode command), and CA and PA increment will return to its normal condition.

(28) SET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[4]=1, CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

Set Cursor Update mode is used to turn ON the Cursor Update mode function. AC[4] will be set to 1 and register CR will be set to the value of register CA.

When AC[4]=1, column address (CA) will only increase with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support "Read-Modify-Write" for cursor implementation.

(29) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(double-byte command)	1	0	CEN [7:0] register parameter							

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-pages in the LCD. Default : **159**.

(30) SET PARTIAL DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(double-byte command)	1	0	DST [7:0] register parameter							

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. Default value: **0**.

(31) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(double-byte command)	1	0	DEN [7:0] register parameter							

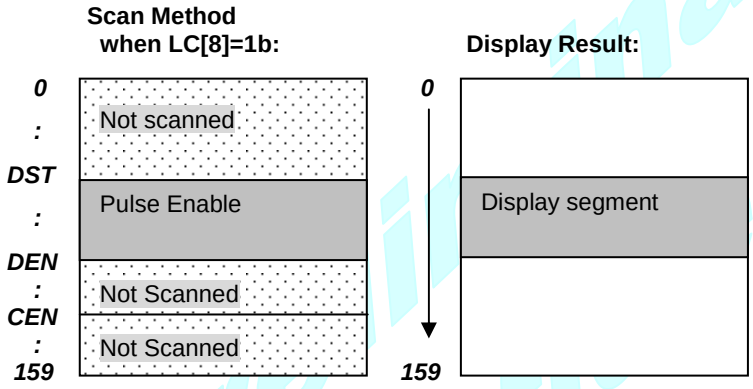
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. Default value: **159**.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1b, the Mux-Rate is narrowed down to DEN-DST+1. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted. When Mux-Rate is under 41, it is recommend to set BR=6.

For minimum power consumption, set LC[8]=1b, set (DST, DEN, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use B/W mode, set PC[0]=0b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(32) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (double -byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	1	0	WPC0[7:0] register parameter							

This command is to program the starting column address of RAM program window.

(33) SET WINDOW PROGRAM STARTING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	1	0	**0**	**0**	WPP0[5:0] register parameter					

This command is to program the starting Page Address of RAM program window.

(34) SET WINDOW PROGRAM ENDING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (double -byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	1	0	WPC1[7:0] register parameter							

This command is to program the ending column address of RAM program window.

(35) SET WINDOW PROGRAM ENDING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	1	0	**0**	**0**	WPP1[5:0] register parameter					

This command is to program the ending Page Address of RAM program window.

(36) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program. Default value of AC3: **0: Disable**.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and PA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), PID (AC[2]), auto-increment order (AC[1]) and MX (LC[0]) register setting. WA decides whether the program RAM address advances to next page / column after reaching the specified window column / page boundary. PID controls the RAM address increasing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address increasing from 159-WPC0 to 159-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

Display Data Direction	Function Setting			Image in Display Data Ram (Start : ●) (Physical origin: upper left corner)
	AIO AC[1]	MX LC[0]	RID AC[2]	
Normal	0	0	0	
Y-mirror	0	0	1	
X-mirror	0	1	0	
X-mirror Y-mirror	0	1	1	

(37) SET MTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	1	0	**0**	**0**	**0**	MTPC[4:0] register parameter				

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Idle 001 : MTP Read
010 : MTP Erase 011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable, automatically cleared each time after MTP command is done. Default: 0b
MTPC[4] : MTP value valid. Ignore MTP value when L. Default: 1b

■ The following commands (38)~(42) are only valid when MTPC[3] =1:

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

(38) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	1	0	**0**	**0**	MTPM[5:0] register parameter					

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[5:0]: Set PMO value. Default: 00H.

This command is only valid when MTPC[3]=1.

(39) SET MTP READ POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set RV (Triple-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**
	1	0	RV[7:0] register parameter							

This command is for fine tuning V_{LCD} for MTP-Read (with BR=00) and is valid only when MTPC[3]=1. Default: 00H.

(40) SET MTP PROGRAM/ERASE POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WV (double-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**
	1	0	WV[7:0] register parameter							

This command is for fine tuning V_{LCD} for MTP-Program/Erase (with BR=10) and is valid only when MTPC[3]=1. Default: 16H.

(41) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WT (double -byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**
	1	0	WT[7:0] register parameter							

This command is only valid when MTPC[3]=1. Default: 60H.

(42) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set RT (double-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**
	1	0	RT[7:0] register parameter							

This command is only valid when MTPC[3]=1. Default: 04H.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1638c via registers CEN, DST, DEN, and partial display control LC[9:8].

Combined with low power partial display mode and a low bias ratio of 6, UC1638c can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$BR = V_{LCD}/V_{BIAS}$,
where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=160), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to loose visibility.

UC1638c supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	10	11	12

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	4	5	6	7
% per ^{o}C	-0.00	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[0].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\,\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Gray shade LCD is sensitive to even a 1.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

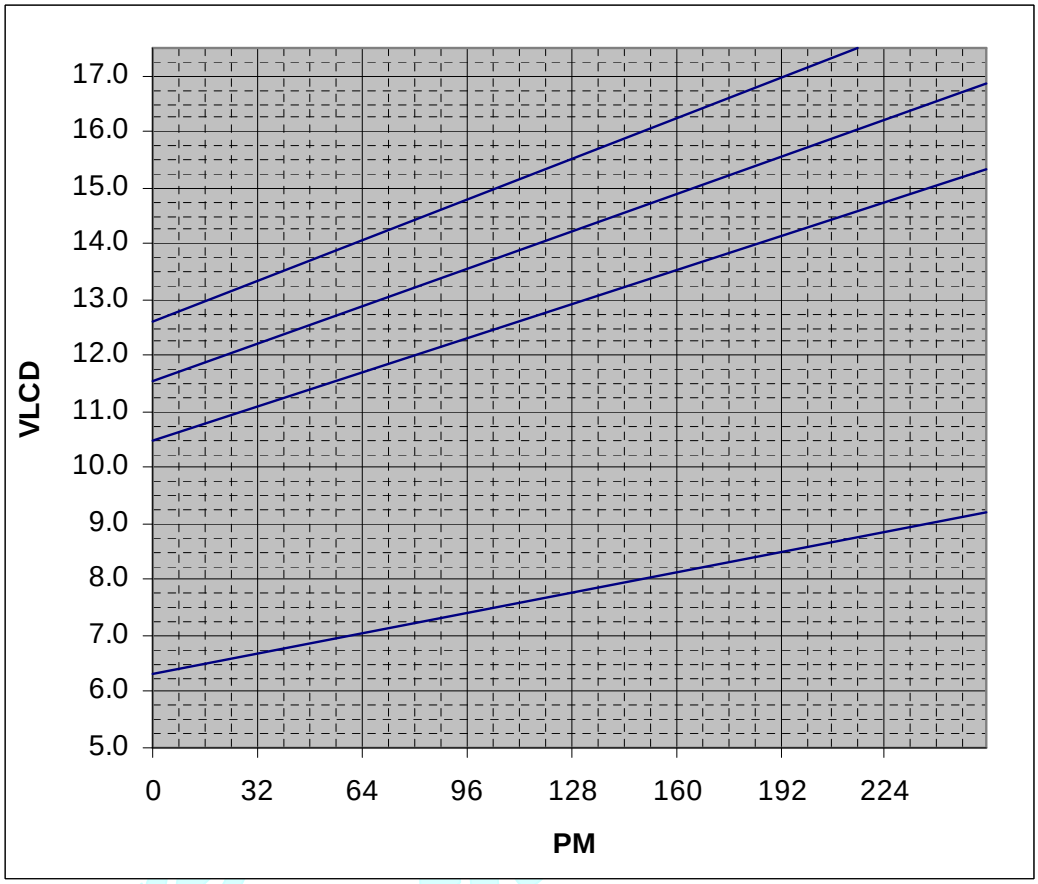
UC1638c provides a V_{LCD} fine-tuning function by adding a variable resistor between Vr and Ground, ranging from $0\,\Omega$ to $500K\,\Omega$. V_{LCD} adjustable range is $\pm 3\%$. Yet, the result of V_R adjustment is still limited in between PM=0 ~ PM=255.

For the best results, software or MTP-based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1638c is designed to handle LCD panels with load capacitance up to ~15nF when V_{DD2} = 2.7V. 15nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels, use higher V_{DD}.

V_{LCD} QUICK REFERENCE



V_{LCD} Relationship to BR and PM at 25 °C

BR	C_{V0} (V)	CPM (mV)	PM	V_{LCD} (V)
6	6.300	11.34	0	6.30
			255	9.19
10	10.500	18.90	0	10.50
			255	15.32
11	11.550	20.79	0	11.55
			255	16.85
12	12.600	22.68	0	12.60
			216	17.50

Note:

1. For good product reliability, keep $V_{LCD(MAX)}$ under **17.5V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

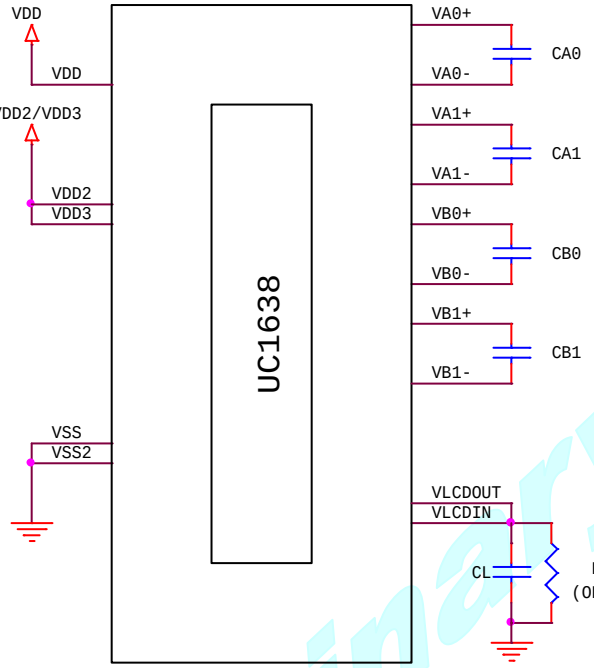


FIGURE 1.a: Reference circuit using INTERNAL Hi-V generator circuit

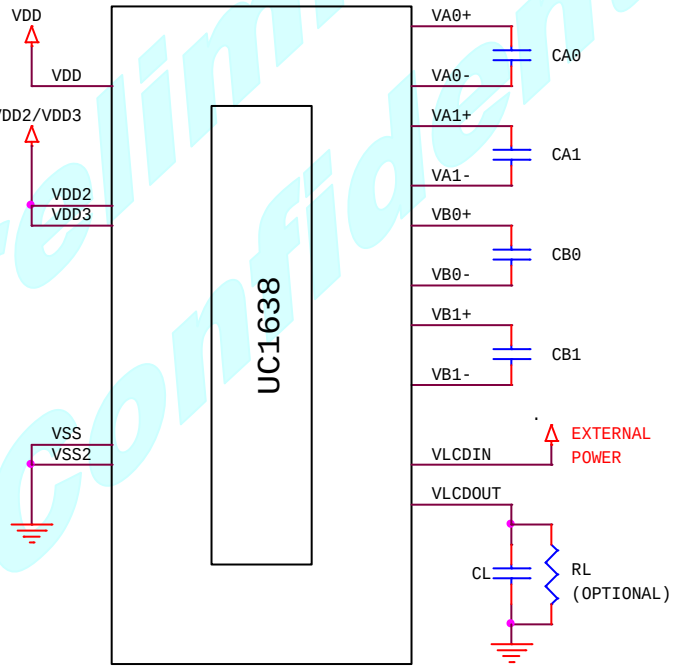


FIGURE 1.b: Reference circuit using EXTERNAL Hi-V generator circuit

Sample component values:

C_{AX}, C_{BX}: For panels of 3-inch or smaller, use 2.2uF capacitor;
For panels bigger than 3 inches, use 5µF capacitor or higher.
(Capacitor size depends on panel capacitance loading and actual image performance.)

C_L: 330nF (25V) is appropriate for most applications.

R_L: 3.3M Ω ~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

Note:
The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1638c contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 109, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 108, 80, 56 and 40, line rate will be scaled down by 1.5, 2, 3 and 4 times automatically to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When fast LC material with ($t_r + t_f$) < 160mS is used, faster line rate may be required under 4-shade mode to maintain good contrast ratio at operating temperature >50^{o}C.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are shorted to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~160, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1638c will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1638c will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1638c provides flexible control of Mux Rate and active display area. Please refer to related Command Description for more detail.

GRAY-SHADE MODULATION

UC1638c uses a proprietary line rate modulation scheme to generate 8 levels of gray shade. The relative levels of the gray shades can be programmed by setting register bit LC[7:5]. It controls the relative position of the light gray and dark gray shades. For detailed value, please refer to the register definition table.

ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1638c can be as short as 30µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize V_{DD}, V_{SS} noise, and ensure sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

COM TRACE

Excessive RC decay of COM scanning pulse can cause fluctuation of contrast and increase the crosstalk of COM direction.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 1.8\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 0.44\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

SEG TRACE

Excessive RC decay of SEG signal can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.5\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD}/#_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10}) / V_{10} = (V_{ON}-V_{OFF}) / V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics. V90 and V10 refers to the applied voltage required to achieve 90% and 10% of the ultimate transmission at saturating voltages respectively.

And V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/160	1/12	7.93%	6.3%	5.7%
1/160	1/11	7.77%	6.2%	5.6%

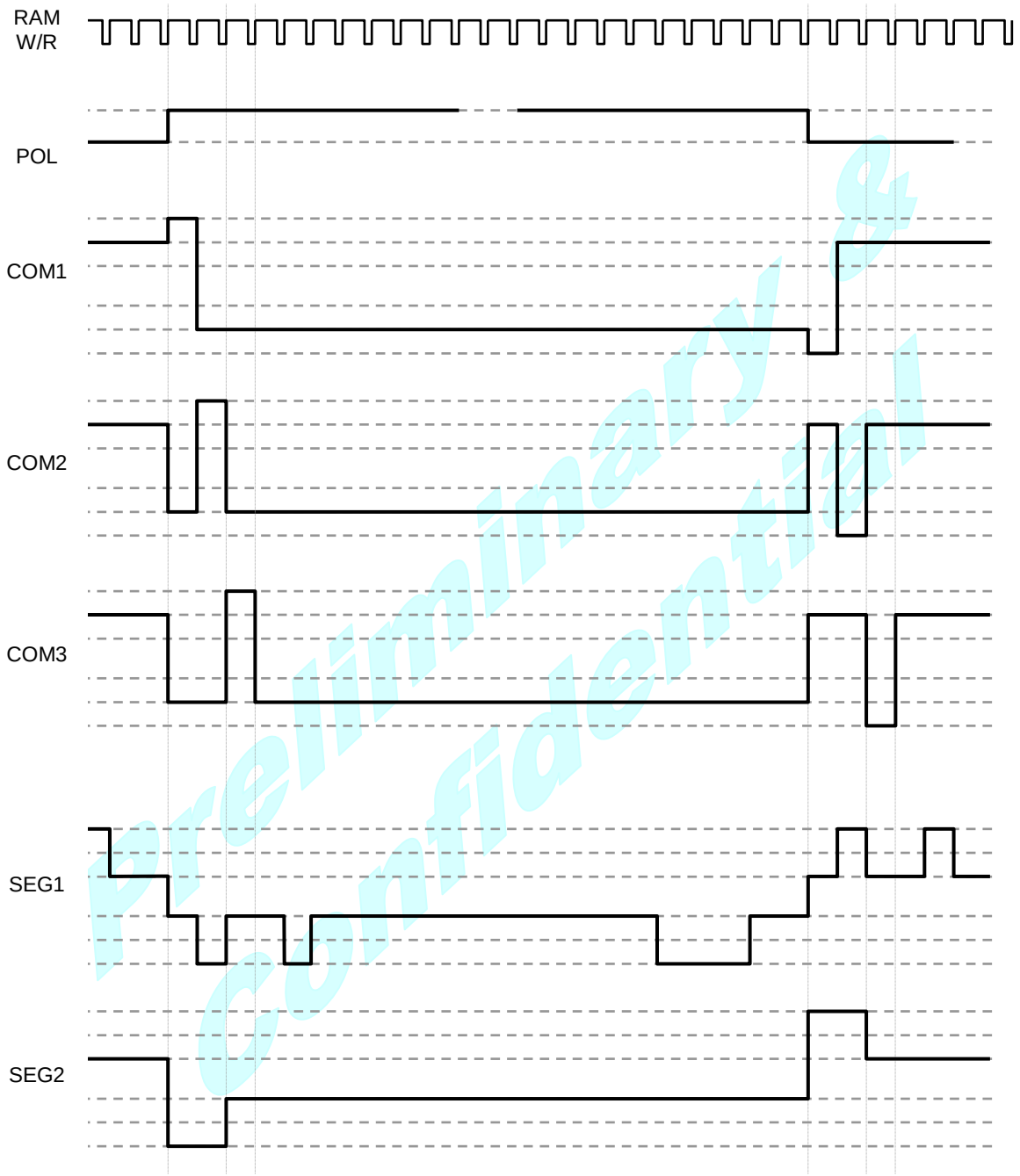


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1638c supports 2 parallel bus protocols in 8-bit bus width, and 3 serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type				
		Parallel		Serial		
		8080	6800	S8 (4-wire)	S9 (3-wire)	I^2C (2-wire)
Width		8-bit	8-bit	–		
Access		Read (data and status) / Write				Write
Control & Data Pins	BM[1:0]	10	11	00	01	00
	CS[1:0]	Chip Select				A[3:2]
	CD	Control/ Data				0
	WR0	$\overline{WR}$	R/ $\overline{W}$	0		
	WR1	$\overline{RD}$	EN	0		
	DB[7:6]	Data	Data	ACK		–
	DB[5:3]	Data	Data	DB5/DB4=SDAO, DB3=SDAI		
	DB[2]	Data	Data	–		
	DB[1]	Data	Data	0	1	1
	DB[0]	Data	Data	SCK		

* Connect unused control pins and data bus pins to V_{SS}.

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1638c internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, by either `Set CA`, or `Set PA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port DB[7].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT BUS OPERATION

UC1638c supports 8-bit bus width.

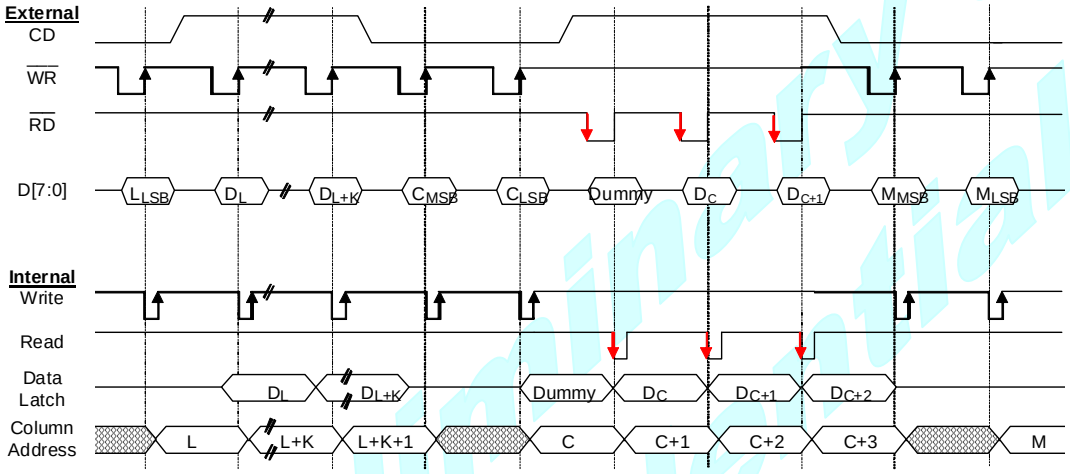


FIGURE 3: 8-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1638c supports 3 serial modes, a 4-wire SPI mode (S8), a compact 3-wire SPI mode (S9), and a 2-wire SPI mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and DB[1]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Read status and write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

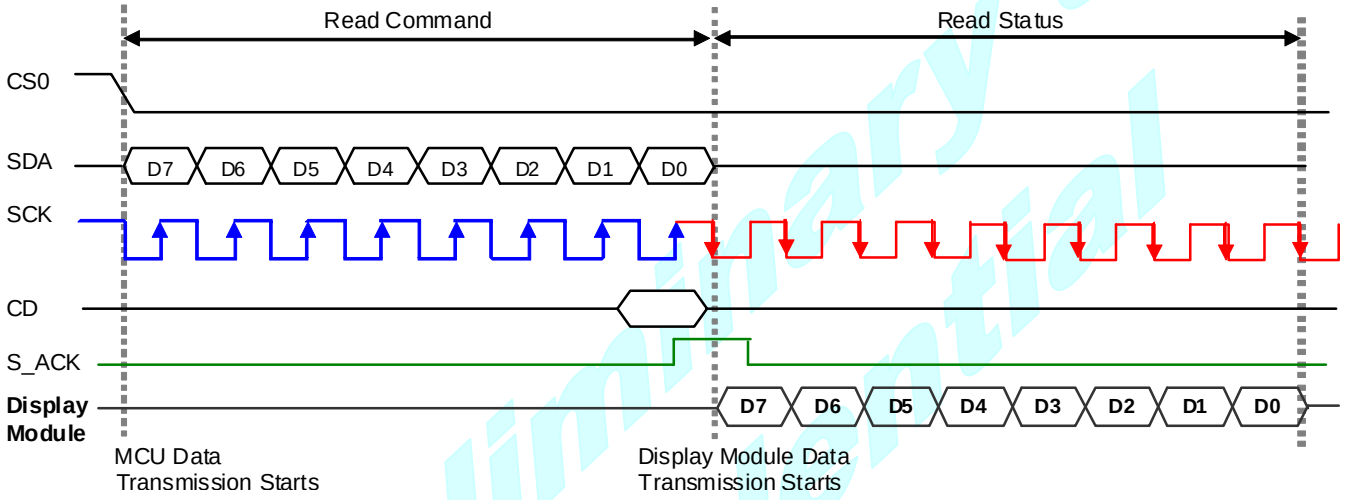


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

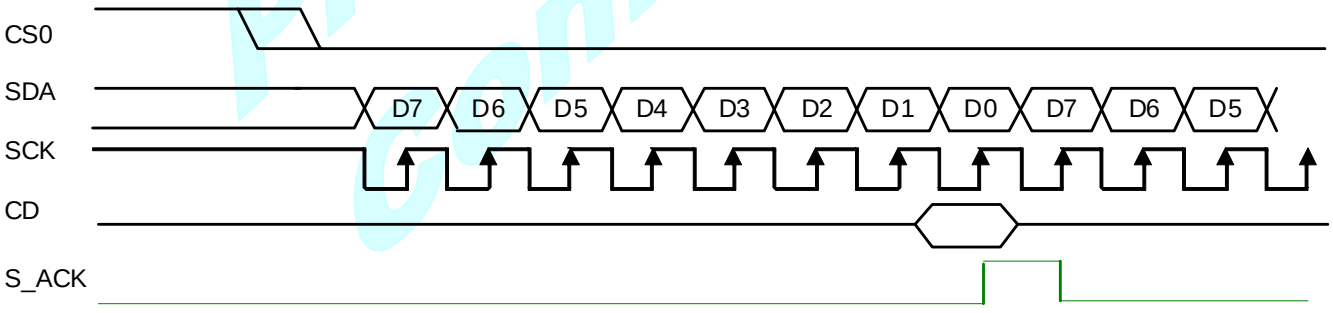


FIGURE 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIRE) INTERFACE

Read status and write operations are supported in this 3-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data or command is recommended but optional.

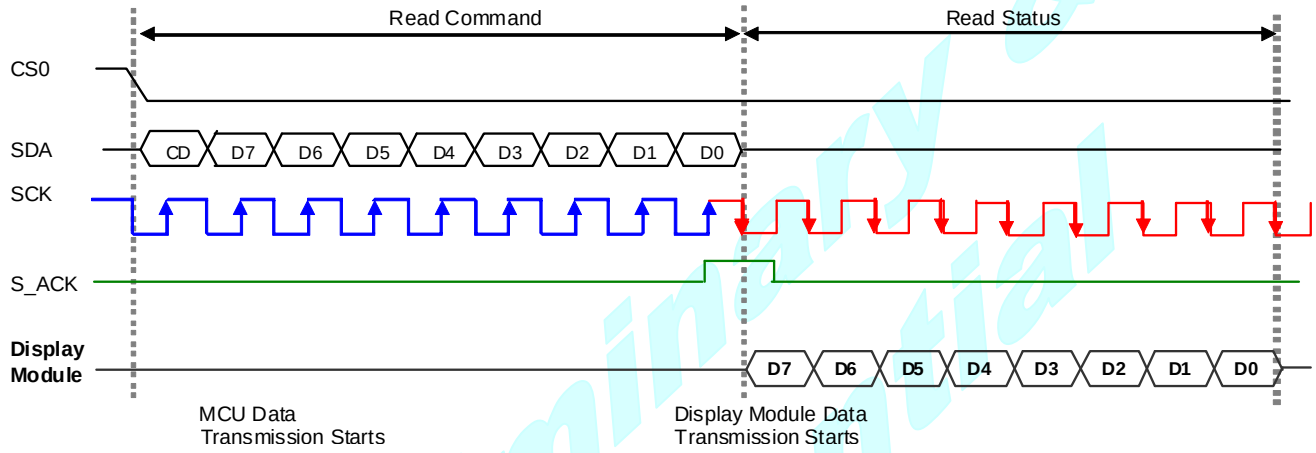


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

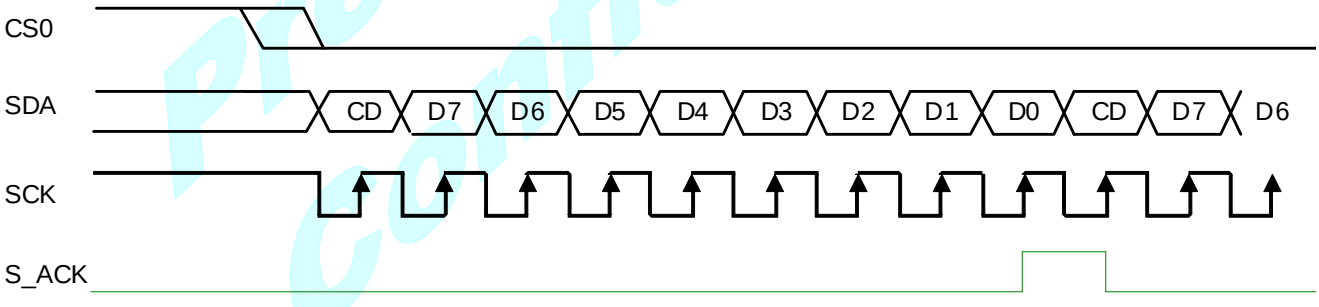


FIGURE 5.b: 3-wire Serial Interface (S9) – Write

2-WIRE SERIAL INTERFACE (I^2C)

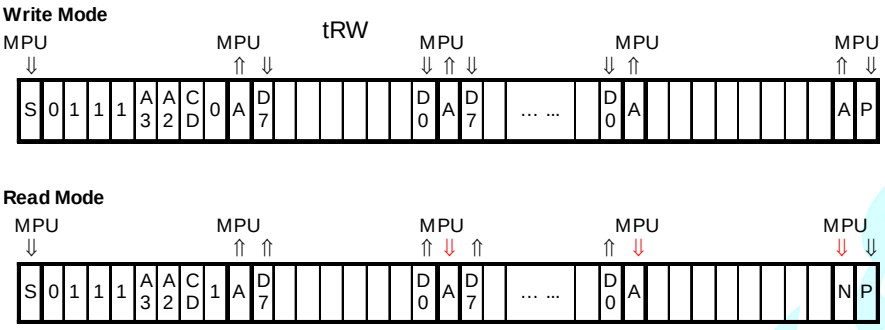


FIGURE 6: 2-wire Serial Interface (I2C)

When BM[1:0] is set to “LL” and DB1 are set to ”H”, UC1638c is configured as a I^2C Bus signaling protocol compliant slave device. Please refer to I^2C standard for details of the bus signaling protocol. Please refer to AC Characteristic section for timing parameters of UltraChip’s implementation.

In this mode, pins CS[1:0] become A[3:2] and are used to configure UC1638c’s device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I^2C mode.

Each UC1638c’s I^2C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

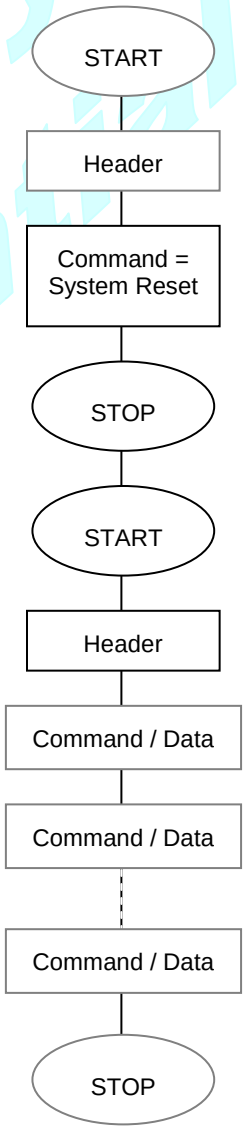
Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I^2C mode and should be connected to V_{SS}.

The direction (read or write) and the content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1638c will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either MCU or UC1368c) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the MCU.

When using I^2C serial mode, if the command of System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a “System Reset” command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

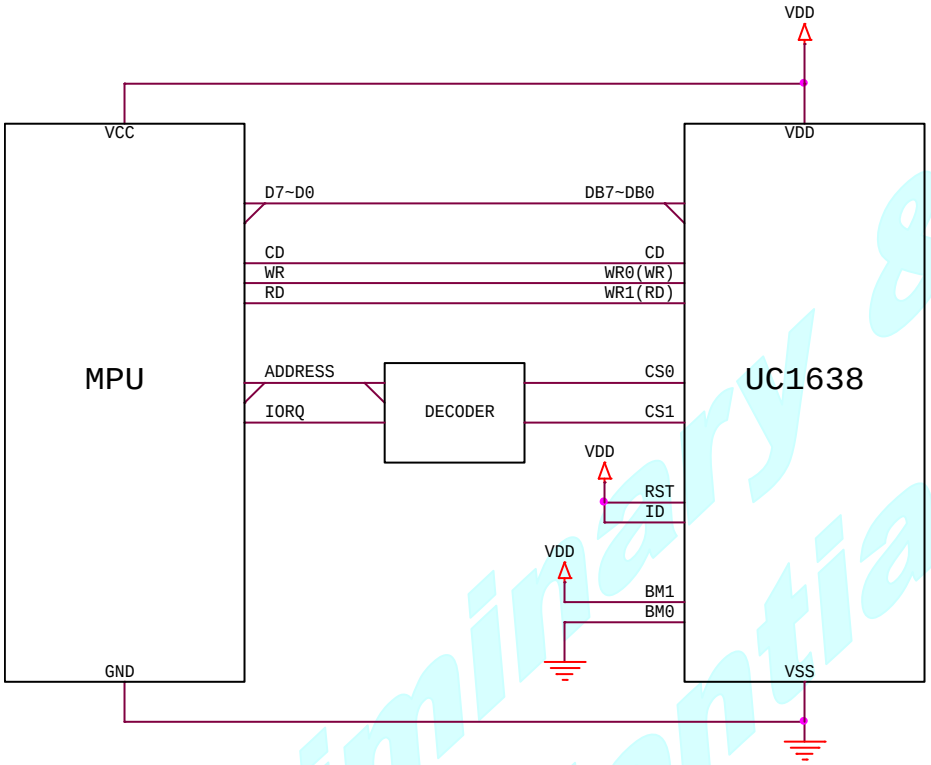


FIGURE 7: 8080/8-bit parallel mode reference circuit

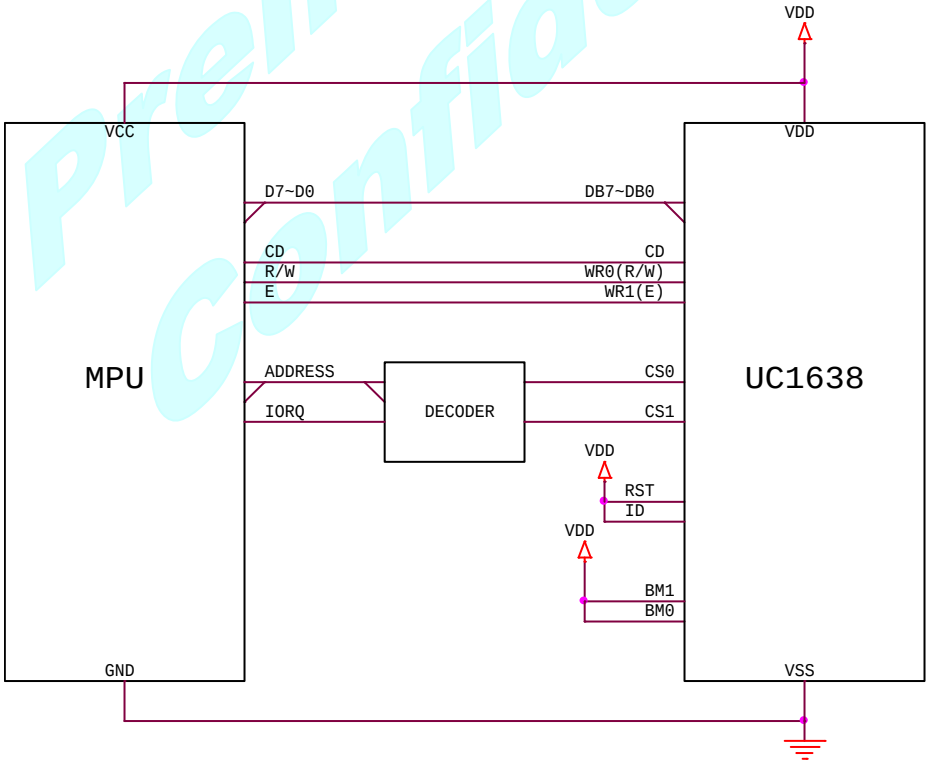


FIGURE 8: 6800/8-bit parallel mode reference circuit

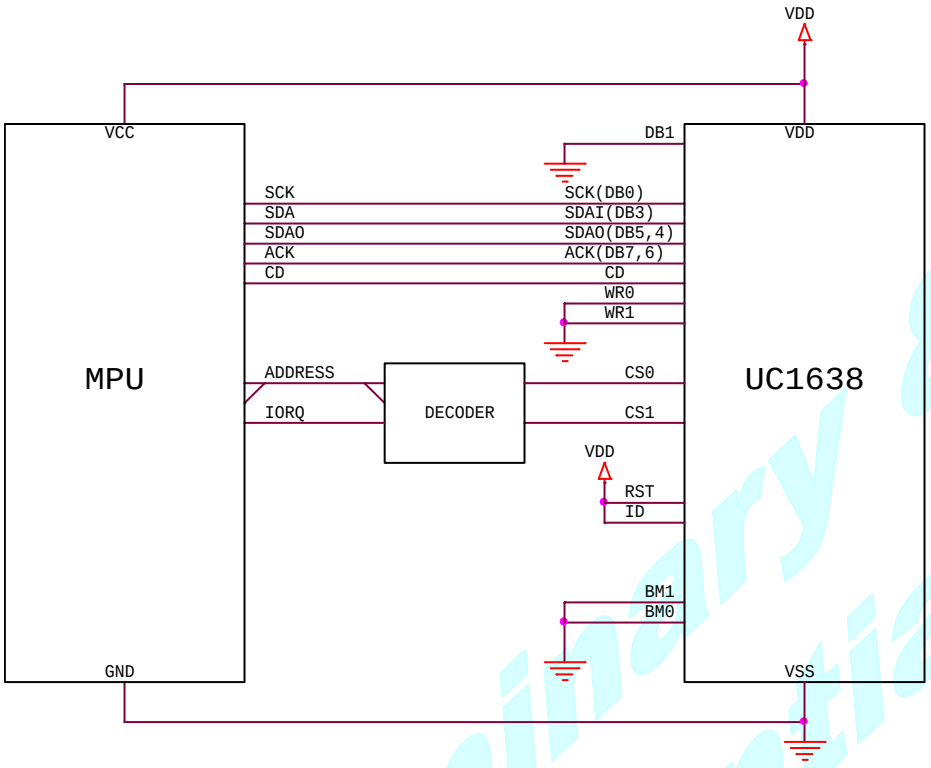


FIGURE 9: 4-Wire SPI (S8) serial mode reference circuit

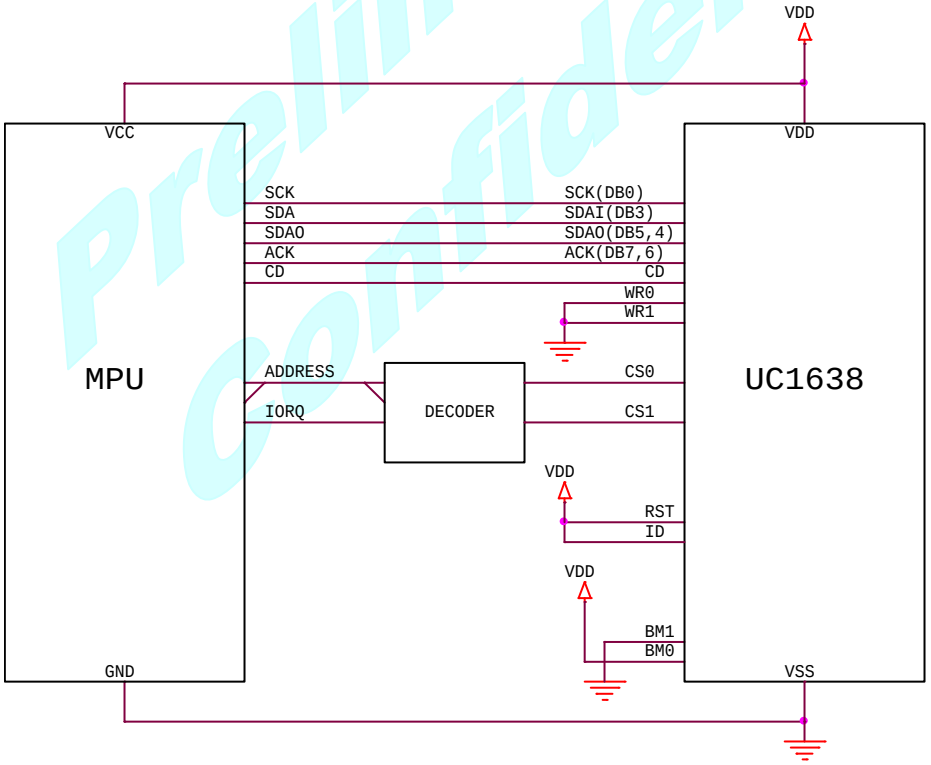


FIGURE 10: 3-Wire SPI (S9) serial mode reference circuit

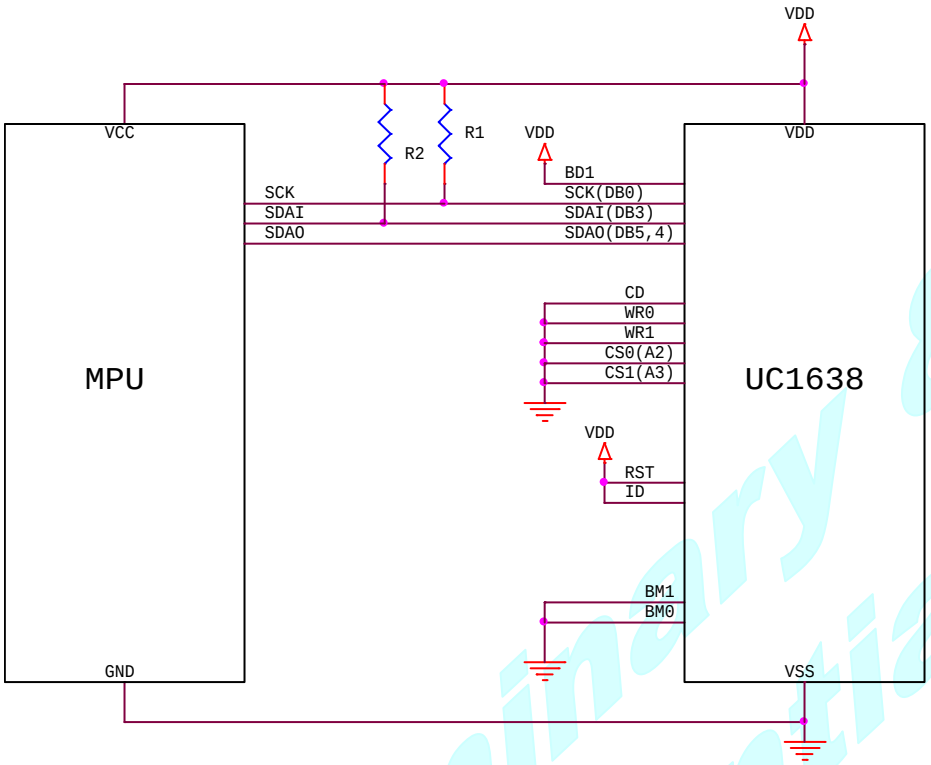


FIGURE 11: 2-Wire SPI (I^2C) serial mode reference circuit

Note:

1. When using Read function:

(8080) Set WR1=0 (6800) Set WR1=1 → data output will be enabled. (Serial) Set SCK=0	(8080) Set WR1=1 (6800) Set WR1=0 → data output will be disabled. (Serial) Set SCK=1

2. It is REQUIRED to set MPU's data port to 1 before Data Read or Status Read actions.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 160x240x2.

After setting CA and PA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and page data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing `Set Page Address` and `Set Page_C Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (159), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of row, CA will be reset to 0 and PA will increase or decrease, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 159), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (239–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, 160)

Where Mod is the modular operator and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *160*. Effects such as row scrolling, row swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX-1*, *160*)
where MUX = CEN + 1

Otherwise
Line = Mod (*Line-1* , *160*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

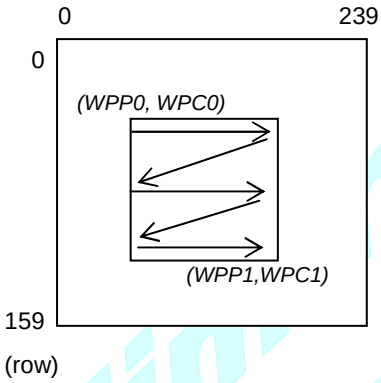
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[3]. After AC[3] sets, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[3] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or page direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

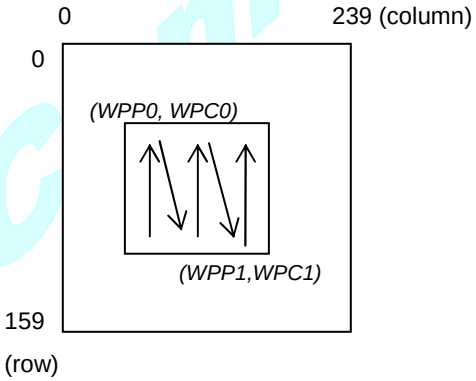
Example1: AC[2:0] = 001, MX=0

(PA auto INCREASING, COLUMN increasing first, auto wrap around, Mirror-X OFF)



Example 2: AC[2:0] = 111 MX = 0

(PA auto DESCREASING, PAGE increasing first, auto wrap around, Mirror-X OFF)



For DC[4:3] = 01b (2-bit per pixel, 4-Shade mode)

Data	Line Addr
D1:0	00H
D3:2	01H
D5:4	02H
D7:6	03H
D1:0	04H
D3:2	05H
D5:4	06H
D7:6	07H
D1:0	08H
D3:2	09H
D5:4	0AH
D7:6	0BH
D1:0	0CH
D3:2	0DH
D5:4	0EH
D7:6	0FH
…	…
D1:0	9CH
D3:2	9DH
D5:4	9EH
D7:6	9FH

RAM

Page0	11	00														
	10	11														
	01	10														
	00	01														
Page1																
Page2																
Page3																
…																
Page39																

MY=0		MY=1	
SL=0	SL=16	SL=0	SL=16
R1	R145	R160	R16
R2	R146	R159	R15
R3	R147	R158	R14
R4	R148	R157	R13
R5	R149	R156	R12
R6	R150	R155	R11
R7	R151	R154	R10
R8	R152	R153	R9
R9	R153	R152	R8
R10	R154	R151	R7
R11	R155	R150	R6
R12	R156	R149	R5
R13	R157	R148	R4
R14	R158	R147	R3
R15	R159	R146	R2
R16	R160	R145	R1
…	…	…	…
R157	R141	R4	R20
R158	R142	R3	R19
R159	R143	R2	R18
R160	R144	R1	R17
		MUX=160	

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8					SEG237	SEG238	SEG239	SEG240
MX=1	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233					SEG4	SEG3	SEG2	SEG1

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

For 8-bit bus width:

Page0, SEG1 : D[7:0] : 00011011b
Page0, SEG2 : D[7:0] : 01101100b

For DC[4:3] = 10b (1-bit per pixel, B/W mode)

Data	Line Addr
D0	00H
D1	01H
D2	02H
D3	03H
D4	04H
D5	05H
D6	06H
D7	07H
D0	08H
D1	09H
D2	0AH
D3	0BH
D4	0CH
D5	0DH
D6	0EH
D7	0FH
…	…
D4	9CH
D5	9DH
D6	9EH
D7	9FH

RAM

1	0							Page0									
1	0																
0	1																
1	1																
1	0							Page1									
0	1																
0	1																
0	0																
								Page2									
								Page3									
								…									
								Page39									

	MY=0		MY=1	
	SL=0	SL=16	SL=0	SL=16
	R1	R145	R160	R16
	R2	R146	R159	R15
	R3	R147	R158	R14
	R4	R148	R157	R13
	R5	R149	R156	R12
	R6	R150	R155	R11
	R7	R151	R154	R10
	R8	R152	R153	R9
	R9	R153	R152	R8
	R10	R154	R151	R7
	R11	R155	R150	R6
	R12	R156	R149	R5
	R13	R157	R148	R4
	R14	R158	R147	R3
	R15	R159	R146	R2
	R16	R160	R145	R1
	…	…	…	…
	R157	R141	R4	R20
	R158	R142	R3	R19
	R159	R143	R2	R18
	R160	R144	R1	R17
			MUX=160	

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8					SEG237	SEG238	SEG239	SEG240
MX=1	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233					SEG4	SEG3	SEG2	SEG1

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

For 8-bit bus width:

Page0, SEG1 : D[7:0] : 00011011b
Page0, SEG2 : D[7:0] : 01101100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1638c has two different types of Reset:

Power-ON-Reset and *System-Reset*

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by connecting the RST pin to ground.

In the following discussions, Reset means *System Reset*.

The differences between pin reset and software reset are

Procedure (Restoring to default value)	Pin Reset (Power On Reset)	Software Reset
Column Address : CA[7:0]=0	V	V
Page Address : PA[5:0]=0	V	V
RAM Address Control : AC[2:0]=001b	V	V
Other commands expect the 3 commands listed above	V	X

RESET STATUS

When UC1638c enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1638c has three operating modes (OM):
Reset, Sleep, and Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:
Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

The OM changes are synchronized with the edges of UC1638c's internal clock. To ensure consistent system states, wait at least 10µS after issuing the `Set Display Enable` command or triggering `System Reset`.

Action	Mode	OM
RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1638c consumes very little energy in Sleep mode (typically under 5µA).

EXITING SLEEP MODE

UC1638c contains internal logic to check whether V_{LCD} and V_D are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1638c's internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

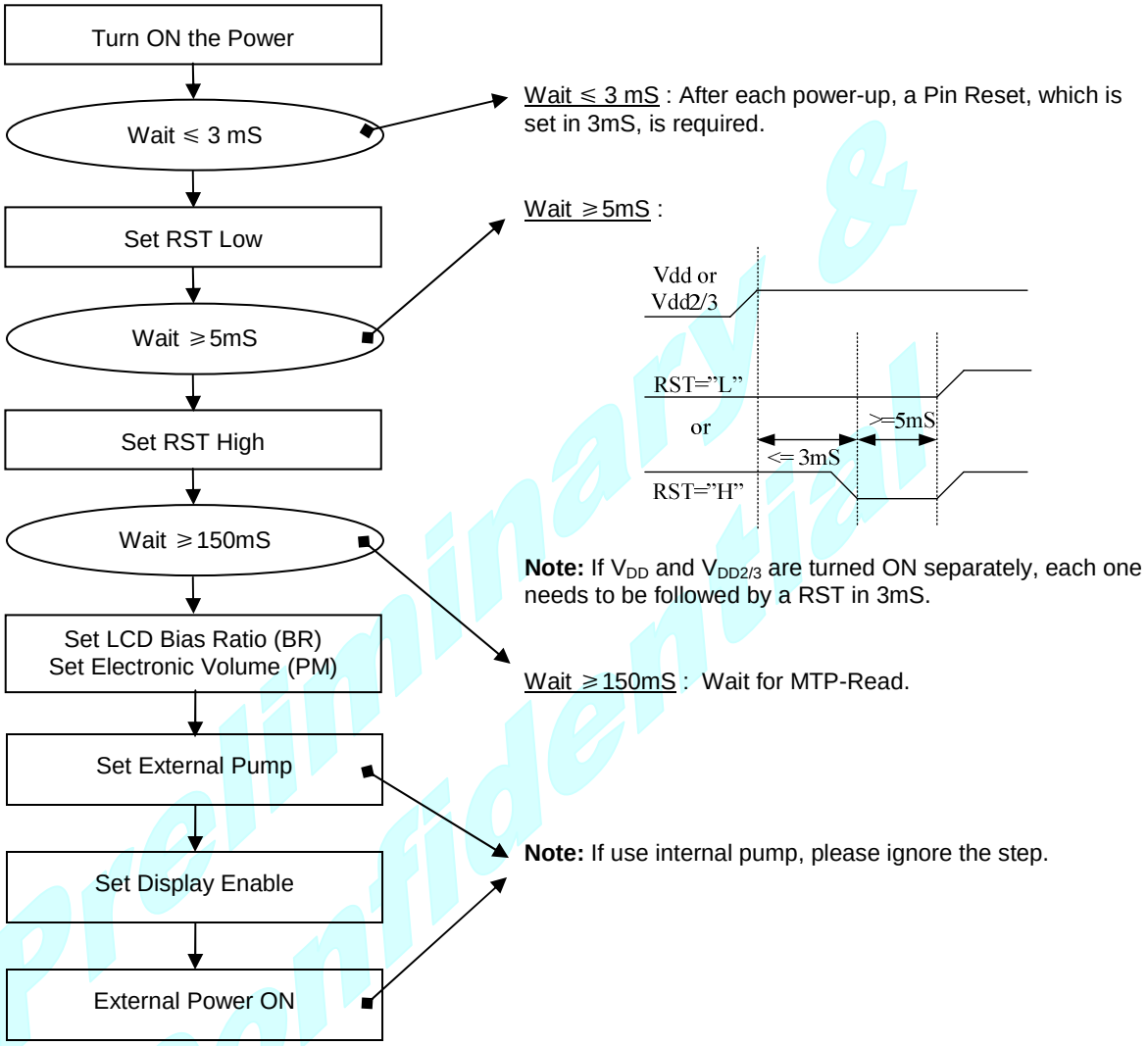


Figure 12: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned on first:

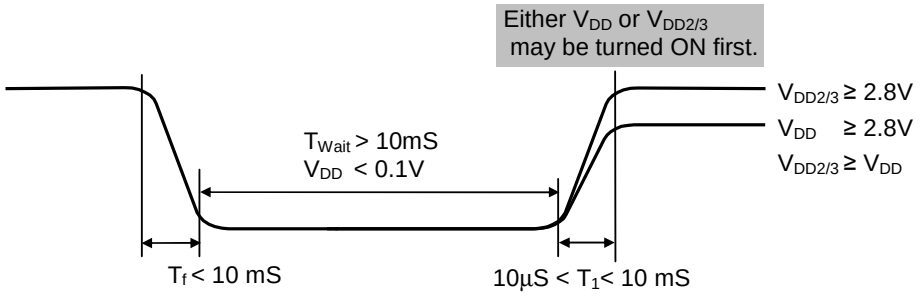
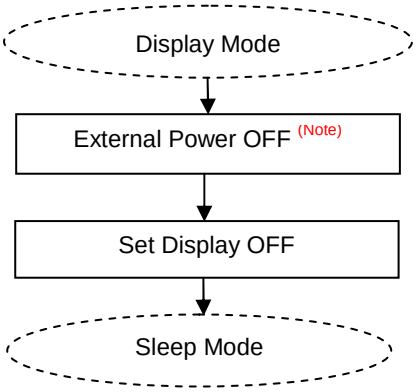


Figure 13: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1638c enters Sleep mode from Display mode by issuing Set Display Disable command.



To exit Sleep mode, issue Set Display Enable.

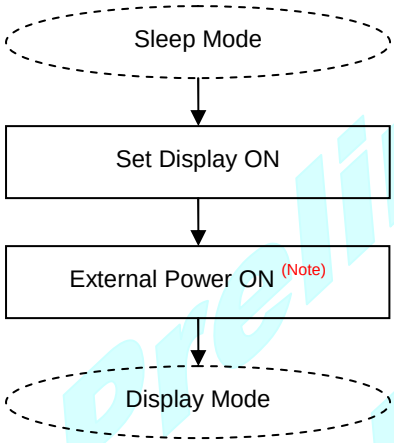


FIGURE 14: Reference Enter/Exit Sleep Mode Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

When internal V_{LCD} is not used, UC1638c will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

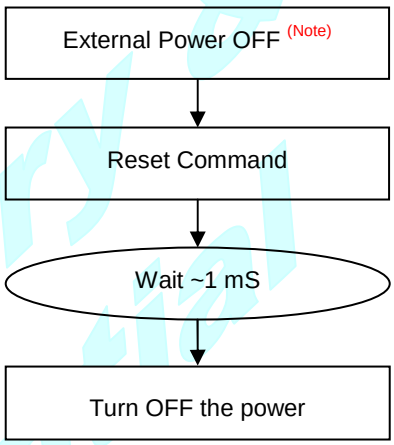


FIGURE 15: Reference Power-Down Sequence

Note: When using internal pump, ignore the “External Power OFF” step.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type
- Required: These items are required
- Customized: These items are not necessary if customer parameters are the same as default
- Advanced: We recommend new users to skip these commands and use default values.
- Optional: These commands depend on what users want to do.

C/D — The type of the interface cycle. It can be either Command (0) or Data (1)

W/R — The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Wait ⩽ 3mS	
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 5mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset	Wait 150mS after RST is High.
C	0	0	0	0	1	0	0	#	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	0	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Gray Shade 2	
C	0	0	1	1	1	0	1	0	#	#	Set Bias Ratio	LCD specific operating voltage setting
R	0 1	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	0	0	0	0	0	0	0	0	0	1	Write display RAM	Set up display image
	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #		
R	0	0	1	1	0	0	1	0	0	1	Set Display Enable	
	1	0	1	0	1	0	1	1	1	1		

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	0	1	System Reset	
	1	0	1	1	1	0	0	0	1	0		
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	0	0	1	0	0	1	Set Display Disable	
	1	0	1	0	1	0	1	1	1	0		
C	0	0	0	0	0	0	0	0	0	1	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #		
R	0	0	1	1	0	0	1	0	0	1	Set Display Enable	
	1	0	1	0	1	0	1	1	1	1		

MULTI-TIME PROGRAM (MTP) NV MEMORY

OVERVIEW

MTP feature is available for UC1638c such that 1LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1638c:

MTP-Erase, MTP-Program, and MTP-Read

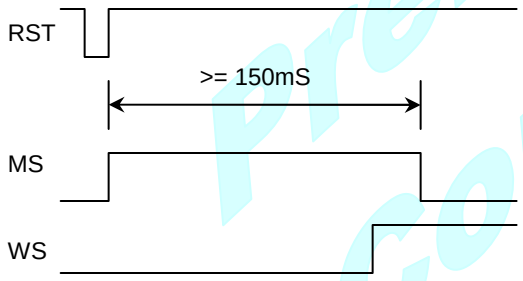
MTP-Program requires an external power source supplied to the TST4 pin. MTP allows program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1638c, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1638c, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the Read Status commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use `Read Status` command in a polling loop to make sure {MS,WS}={0,1} before proceeding with the normal operation, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software RESET command. This enables the ICs to turn on display faster without the delay caused by MTP-Read.

It is recommended to use the software *RESET* for such operation control purpose and use hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP1 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operation, TST4 should be open, or connected to V_{DD3}.

	V_{LCD}	**TST4 (external input)**
Program	MTP2 : 16h (12V)	10V (1mA per bit)
Erase	MTP2 : 16h (12V)	Floating or V_{DD3}
Read	MTP1 : 00h (6.3V)	Floating or V_{DD3}

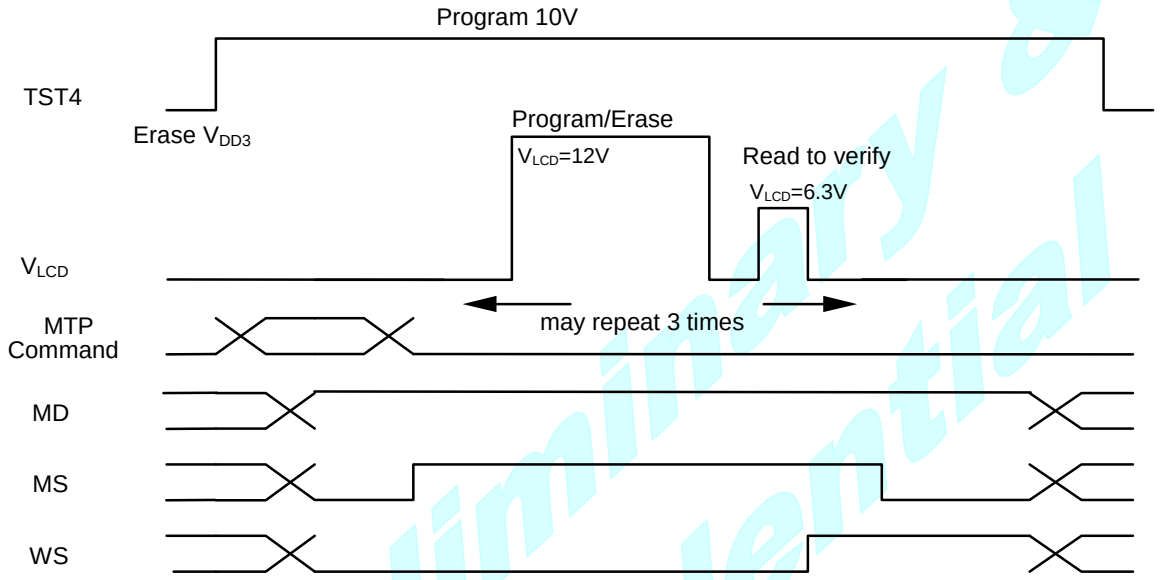
Note:
(1) Do Erase before Program and Program one bit at a time.
(2) When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqslant 3.0V$.

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not.

WS : If the operation succeeded, and current operation will be ended with WS=1.
If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted.

MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

3. MTP Cell Value Usage

There are 6 MTP cell bits. They are divided into two groups for different trimming purpose.

MTP[5:0] : V_{LCD} Trim

When PMO[5]=1: PM with trim = PM - PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.
C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	-	-	-	-	-	-	-	-	-	-	Set RST pin Low	Wait 5 mS after RST is Low
R	-	-	-	-	-	-	-	-	-	-	Set RST pin High	
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON Reset	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[3:2]=11b
R	0	0	1	1	1	1	1	0	1	0	Set RV[7:0] Potentiometer	Set MTP-Read V_{LCD}
	1	0	0	0	0	0	0	0	0	0		MTP1: 00h(6.3V)
R	0	0	1	1	1	1	1	0	1	1	Set WV[7:0] Potentiometer	Set MTP-Write V_{LCD}
	1	0	0	0	0	1	0	1	1	0		MTP2: 16h(12V)
R	0	0	1	1	1	1	1	1	0	0	Set MTP Write Timer	Set MTP Timer
	1	0	0	1	1	0	0	0	0	0		MTP3: 60h(200mS)
R	0	0	1	1	1	1	1	1	0	1	Set MTP Read Timer	Set MTP Timer
	1	0	0	0	0	0	0	1	0	0		MTP4: 04h(35mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	1	0	-	-	0	0	0	0	0	1	MTPM	Ex: To program D0 to be 1, set MTPM to 000001b*
R	-	-	-	-	-	-	-	-	-	-		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
	1	0	0	0	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	0	0	0	0	0	0	0	1	1	Get Status & PM	Check MTP Status until MS=0 and WS=1
	1	1	-	-	-	-	-	WS	-	MS		
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	-	-	-	-	-	-	-	-	-	-	Set RST pin Low	Wait 5 mS after RST is Low
R	-	-	-	-	-	-	-	-	-	-	Set RST pin High	
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON Reset	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[3:2]=11b
R	0	0	1	1	1	1	1	0	1	0	Set RV[7:0] Potentiometer	Set MTP-Read V_{LCD}
	1	0	0	0	0	0	0	0	0	0		MTP1: 00h(6.3V)
R	0	0	1	1	1	1	1	0	1	1	Set WV[7:0] Potentiometer	Set MTP-Erase V_{LCD}
	1	0	0	0	0	1	0	1	1	0		MTP2: 16h(12V)
R	0	0	1	1	1	1	1	1	0	0	Set MTP Write Timer	Set MTP Timer
	1	0	0	1	1	0	0	0	0	0		MTP3: 60h(200mS)
R	0	0	1	1	1	1	1	1	0	1	Set MTP Read Timer	Set MTP Timer
	1	0	0	0	0	0	0	1	0	0		MTP4: 04h(35mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	1	0	0	0	1	1	1	1	1	1	MTPM	Ex: To erase D[7:0], set MTPM to 111111b*
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
	1	0	0	0	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	0	0	0	0	0	0	0	1	1	Get Status & PM	Check MTP Status until MS=0 and WS=1
	1	1	-	-	-	-	-	WS	-	MS		
R											V_{DD}=0V	Power OFF

* It is recommended that users clear all the bits to be programmed.

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

Machine Mode		Human Body Mode	
V_{DD} mode	V_{SS} mode	V_{DD} mode	V_{SS} mode
(TBD)	(TBD)	(TBD)	(TBD)

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1 and 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Generated voltage (-30^{O}C ~ +85^{O}C)	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.7	2.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.7	2.8~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.7V, 25^{O}C		14.5	17.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.7V, 25^{O}C	0.99		1.59	V
V_{IL}	Input logic LOW				0.2V_{DD}	V
V_{IH}	Input logic HIGH		0.8V_{DD}			V
V_{OL}	Output logic LOW				0.2V_{DD}	V
V_{OH}	Output logic HIGH		0.8V_{DD}			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85 ^{o}C			50	µA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{0N(SEG)}$	SEG output impedance	V_{LCD} = 17.5V		1.20	1.70	kΩ
$R_{0N(COM)}$	Upward COM output impedance	V_{LCD} = 17.5V		1.20	1.70	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	26.0	+10%	klps

POWER CONSUMPTION

V_{DD} = (TBD) V, Bias Ratio = (TBD)b , PM = (TBD),
V_{LCD} = (TBD)V, Line Rate = (TBD) Klps, Mux Rate = (TBD) ,
Bus mode = (TBD), C_L = (TBD)nF, C_B = (TBD)µF,
Temperature = 25^{O}C, All HV outputs are open circuit.

Display Pattern	Conditions	Typical	Maximum	Unit
All-OFF	Bus = idle	(TBD)	(TBD)	µA
All-ON	Bus = idle	(TBD)	(TBD)	µA
2-pixel checker	Bus = idle	(TBD)	(TBD)	µA
-	Reset (standby current)	< 3	5	µA

AC CHARACTERISTICS

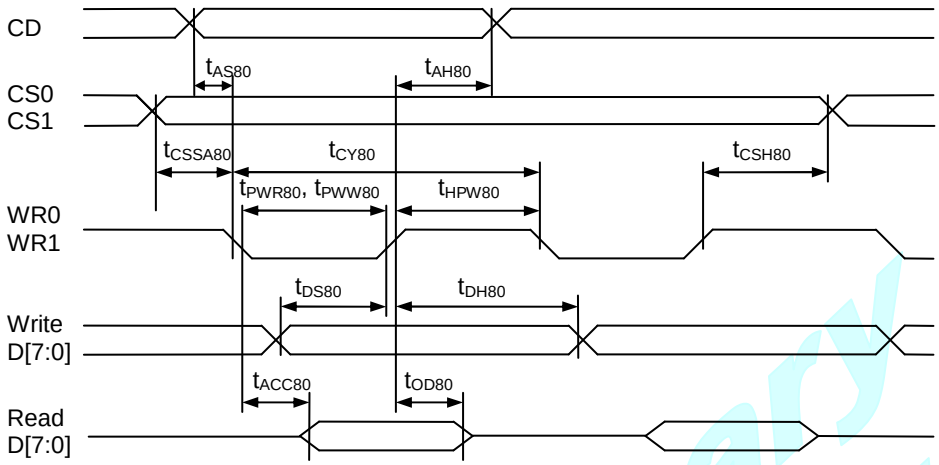


FIGURE 16: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY80}	WR0, WR1	System cycle time		350 / 280	–	nS
t_{PWR80}		Pulse width		160 / --		
t_{PWW80}		Pulse width		-- / 125		
t_{HPW80}		High pulse width		160 / 125		
t_{DS80} t_{DH80}	Write D7~D0	Data setup time Data hold time		-- / 45 -- / 10	–	nS
t_{ACC80} t_{OD80}	Read D7~D0	Read access time Output disable time	C_L = 100pF	– / -- 100 / --	150 –	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

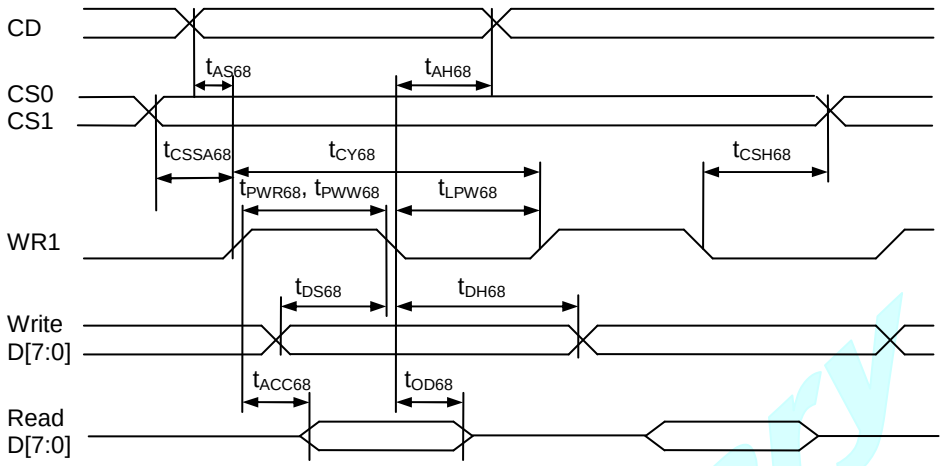


FIGURE 17: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY68}	WR0, WR1	System cycle time		350 / 280	–	nS
t_{PWR68}		Pulse width		160 / –-		
t_{PWW68}		Pulse width		–- / 125		
t_{LPW68}		High pulse width		160 / 125		
t_{DS68} t_{DH68}	Write D7~D0	Data setup time Data hold time		-- / 45 -- / 10	–	nS
t_{ACC68} t_{OD68}	Read D7~D0	Read access time Output disable time	C_L = 100pF	– / -- 100 / --	150 –	nS

Note: tr (rising time), tf (falling time) : ⩽ 15nS

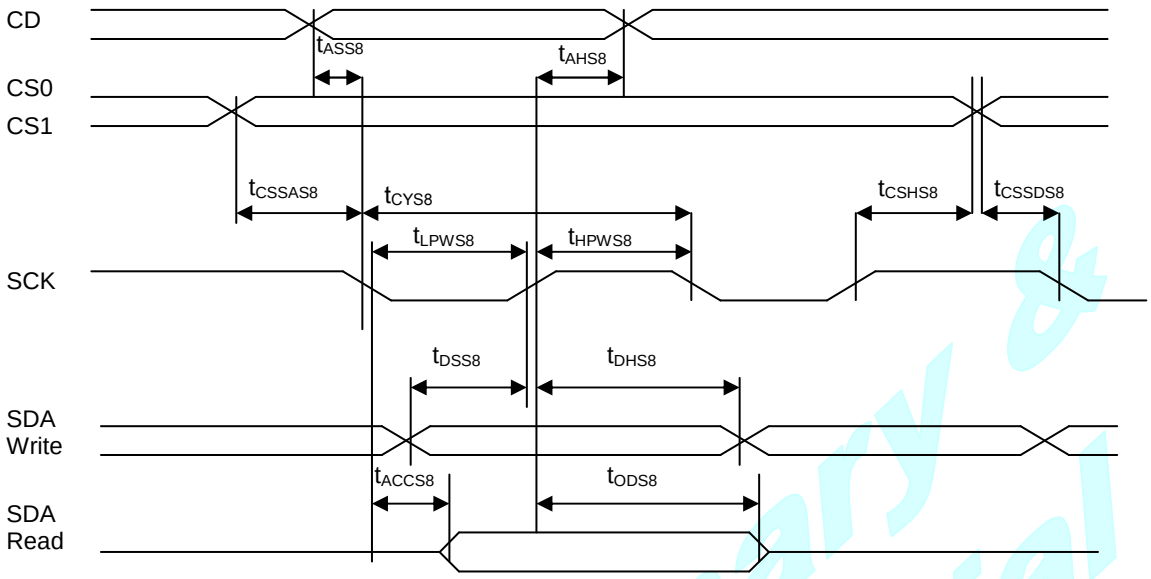


FIGURE 18: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		30		
t_{CSSAS8}	CS1/CS0	Chip select setup time		5	–	nS
t_{CSHS8}		Chip select hold time		30		
t_{CYS8}	SCK	System cycle time		250 / 220	–	nS
t_{LPWS8}		Low pulse width		110 / 95		
t_{HPWS8}		High pulse width		110 / 95		
t_{DSS8}	SDA (Write)	Data setup time		-- / 25	–	nS
t_{DHS8}		Data hold time		-- / 30		
t_{ACCS8}	SDA (Read)	Read access time	C_L = 100pF	– / --	110	nS
t_{ODS8}		Output disable time		80 / --	–	

Note: tr (rising time), tf (falling time) : ≤ 15nS

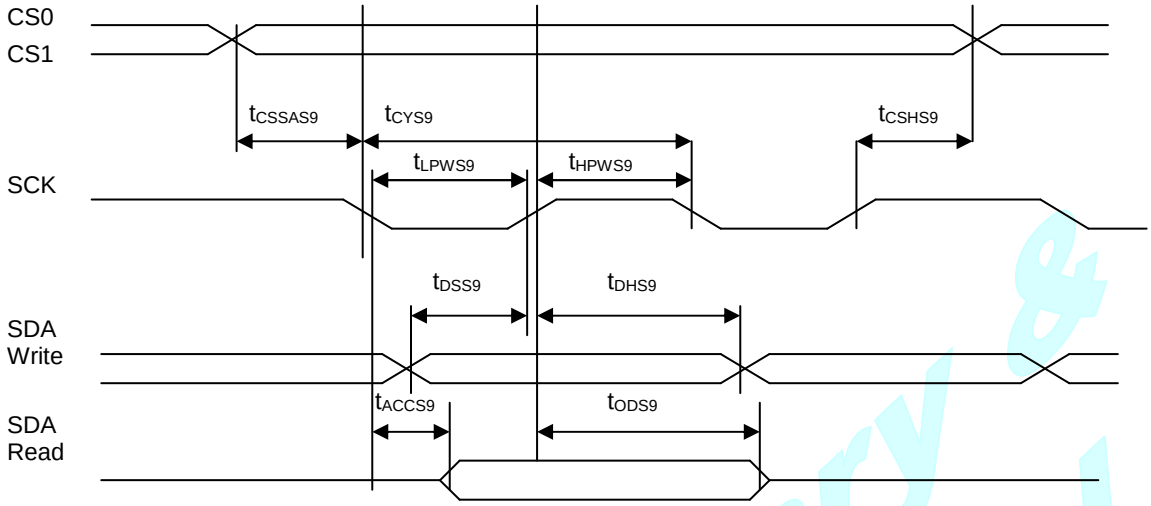


FIGURE 19: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –30 to +85°C)				(read / write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time Chip select hold time		5 30	–	nS
t_{CYS9}	SCK	System cycle time		250 / 220	–	nS
t_{LPWS9}		Low pulse width		110 / 95		
t_{HPWS9}		High pulse width		110 / 95		
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		-- / 25 -- / 30	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / -- 80 / --	110 –	nS

Note: tr (rising time), tf (falling time) : ⩽ 15nS

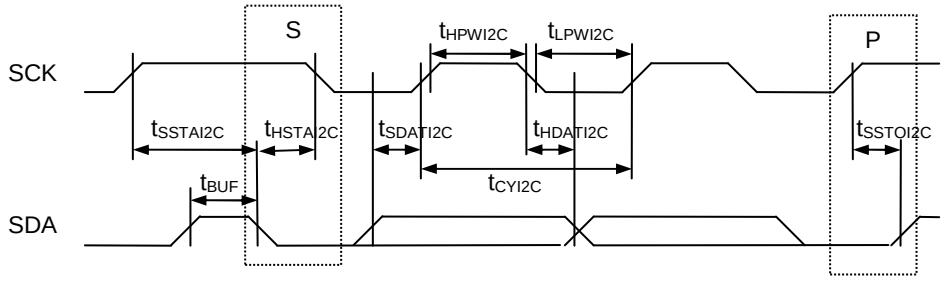


FIGURE 20: Serial Bus Timing Characteristics (for I^2C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C}	SCK	SCK cycle time		530 / 180	–	nS
t_{LPWI2C}		Low pulse width		250 / 90	–	nS
t_{HPWI2C}		High pulse width		250 / 60	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		35	–	nS
t_{HDAI2C}		Data hold time		0	–	nS
$t_{SSTAI2C}$		START Setup time		0	–	nS
$t_{HSTAI2C}$		START Hold time		35	–	nS
$t_{SSTOI2C}$		STOP setup time		0	–	nS
t_{BUF}		Bus Free time between STOP and START condition		75	–	nS

Note: tr (rising time), tf (falling time) : ⩽ 15nS

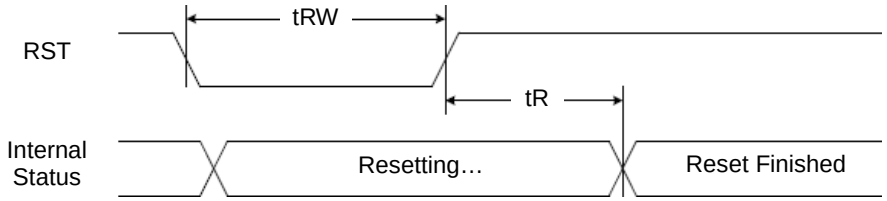
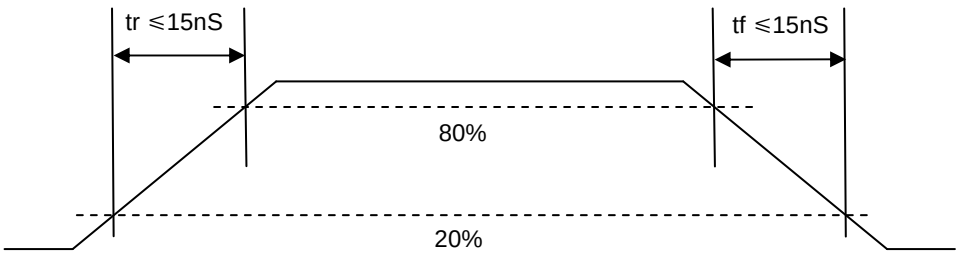


FIGURE 21: Reset Characteristics

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –30 to +85°C)						
t_{RW}	RST	Reset low pulse width		5	–	mS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		10	–	uS
		Wait before Power Down		1	–	mS

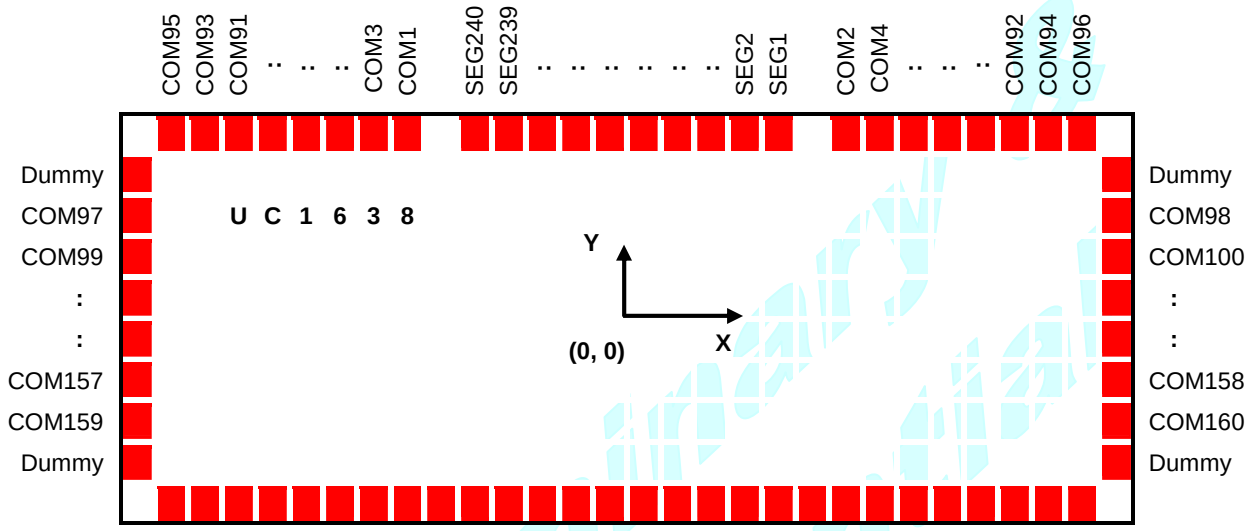
Note:

For each mode, the signal's rising and falling times (tr, tf) are stipulated to be equal to or less than 15nS each.



PHYSICAL DIMENSIONS

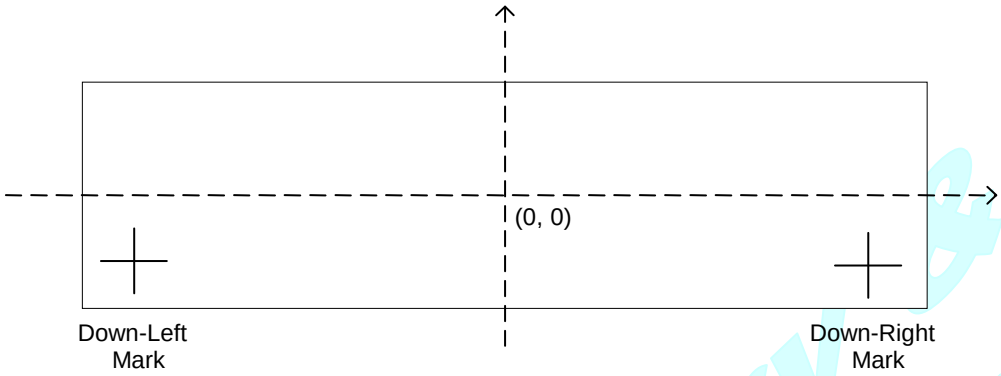
Circuit / Bump View:



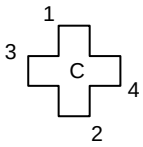
Die / Bump Information:

Die Size:	(9730µM ± 40µM) x (1030µM ± 40µM)	Bump Size:	15µM x 135µM
Die Thickness:	400µM ± 20µM	Bump Pitch:	27µM
Die TTV:	$D_{MAX} - D_{MIN} \leqslant 2\mu M$	Bump Gap:	12µM
Hardness:	90Hv ± 25Hv	Shear force:	>5 g/mil^2
Bump Height:	12µM ± 3µM	Coordinate origin:	(0, 0)
	$H_{MAX} - H_{MIN} \leqslant 2\mu M$	Chip center:	(0, 0)
Bump Area:	2025 µM^2	Pad reference:	Pad center

ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

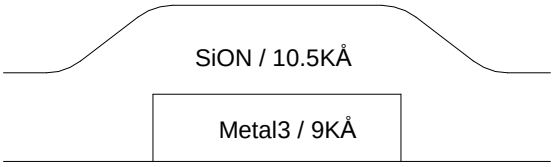
Alignment marks are on Metal3 and under Passivation.

The "+" mark is symmetric both horizontally and vertically.

COORDINATES:

	Down-Left Mark		Down-Right Mark	
	X	Y	X	Y
1	-4592	-398	4572	-398
2	-4572	-458	4592	-458
3	-4612	-418	4552	-418
4	-4552	-438	4612	-438
C	-4582	-428	4582	-428

TOP METAL AND PASSIVATION:



FOR PROCESS CROSS-SECTION

Remark:
Alignment marks are on Metal3 and under Passivation

PAD COORDINATES

#	Pad Name	X	Y	W	H
1	DUMMY1	-4768.5	433	135	15
2	COM<97>	-4768.5	406	135	15
3	COM<99>	-4768.5	379	135	15
4	COM<101>	-4768.5	352	135	15
5	COM<103>	-4768.5	325	135	15
6	COM<105>	-4768.5	298	135	15
7	COM<107>	-4768.5	271	135	15
8	COM<109>	-4768.5	244	135	15
9	COM<111>	-4768.5	217	135	15
10	COM<113>	-4768.5	190	135	15
11	COM<115>	-4768.5	163	135	15
12	COM<117>	-4768.5	136	135	15
13	COM<119>	-4768.5	109	135	15
14	COM<121>	-4768.5	82	135	15
15	COM<123>	-4768.5	55	135	15
16	COM<125>	-4768.5	28	135	15
17	COM<127>	-4768.5	1	135	15
18	COM<129>	-4768.5	-26	135	15
19	COM<131>	-4768.5	-53	135	15
20	COM<133>	-4768.5	-80	135	15
21	COM<135>	-4768.5	-107	135	15
22	COM<137>	-4768.5	-134	135	15
23	COM<139>	-4768.5	-161	135	15
24	COM<141>	-4768.5	-188	135	15
25	COM<143>	-4768.5	-215	135	15
26	COM<145>	-4768.5	-242	135	15
27	COM<147>	-4768.5	-269	135	15
28	COM<149>	-4768.5	-296	135	15
29	COM<151>	-4768.5	-323	135	15
30	COM<153>	-4768.5	-350	135	15
31	COM<155>	-4768.5	-377	135	15
32	COM<157>	-4768.5	-404	135	15
33	COM<159>	-4768.5	-431	135	15
34	DUMMY2	-4768.5	-458	135	15
35	DATA_pad<7>	-4387.8	-424.775	45	82.45
36	DATA_pad<7>	-4327.8	-424.775	45	82.45
37	VDDX	-4267.8	-424.775	45	82.45
38	DATA_pad<6>	-4207.8	-424.775	45	82.45
39	DATA_pad<6>	-4147.8	-424.775	45	82.45
40	DATA_pad<5>	-4087.8	-424.775	45	82.45
41	DATA_pad<5>	-4027.8	-424.775	45	82.45
42	DATA_pad<4>	-3960.2	-424.775	45	82.45
43	DATA_pad<4>	-3900.2	-424.775	45	82.45
44	DATA_pad<3>	-3840.2	-424.775	45	82.45
45	DATA_pad<3>	-3780.2	-424.775	45	82.45
46	DATA_pad<2>	-3712.6	-424.775	45	82.45
47	DATA_pad<2>	-3652.6	-424.775	45	82.45
48	DATA_pad<1>	-3592.6	-424.775	45	82.45
49	DATA_pad<1>	-3532.6	-424.775	45	82.45
50	DATA_pad<0>	-3465	-424.775	45	82.45

#	Pad Name	X	Y	W	H
51	DATA_pad<0>	-3405	-424.775	45	82.45
52	RST_pad	-3334.95	-424.775	45	82.45
53	RST_pad	-3274.95	-424.775	45	82.45
54	CS_pad<0>	-3214	-424.775	45	82.45
55	CS_pad<0>	-3154	-424.775	45	82.45
56	VDDX	-3094	-424.775	45	82.45
57	CS_pad<1>	-3034	-424.775	45	82.45
58	CS_pad<1>	-2974	-424.775	45	82.45
59	CD_pad	-2914	-424.775	45	82.45
60	CD_pad	-2854	-424.775	45	82.45
61	WR_pad<0>	-2794	-424.775	45	82.45
62	WR_pad<0>	-2734	-424.775	45	82.45
63	VDDX	-2674	-424.775	45	82.45
64	WR_pad<1>	-2614	-424.775	45	82.45
65	WR_pad<1>	-2554	-424.775	45	82.45
66	BM_pad<1>	-2494	-424.775	45	82.45
67	BM_pad<1>	-2434	-424.775	45	82.45
68	VDDX	-2374	-424.775	45	82.45
69	BM_pad<0>	-2314	-424.775	45	82.45
70	BM_pad<0>	-2254	-424.775	45	82.45
71	ID_pad	-2194	-424.775	45	82.45
72	ID_pad	-2134	-424.775	45	82.45
73	VDDX	-2074	-424.775	45	82.45
74	POR_DIS_pad	-2014	-424.775	45	82.45
75	POR_DIS_pad	-1954	-424.775	45	82.45
76	VSS	-1894	-424.775	45	82.45
77	VSS	-1834	-424.775	45	82.45
78	VSS	-1774	-424.775	45	82.45
79	VSS	-1714	-424.775	45	82.45
80	VSS	-1654	-424.775	45	82.45
81	VSS	-1594	-424.775	45	82.45
82	VSS	-1534	-424.775	45	82.45
83	VSS	-1474	-424.775	45	82.45
84	VSS	-1414	-424.775	45	82.45
85	VSS	-1354	-424.775	45	82.45
86	VSS	-1294	-424.775	45	82.45
87	VSS	-1234	-424.775	45	82.45
88	VSS	-1174	-424.775	45	82.45
89	VSS	-1114	-424.775	45	82.45
90	VSS	-1054	-424.775	45	82.45
91	VSS	-994	-424.775	45	82.45
92	VSS	-934	-424.775	45	82.45
93	VSS2	-874	-424.775	45	82.45
94	VSS2	-814	-424.775	45	82.45
95	VSS2	-754	-424.775	45	82.45
96	VSS2	-694	-424.775	45	82.45
97	VSS2	-634	-424.775	45	82.45
98	VSS2	-574	-424.775	45	82.45
99	VSS2	-514	-424.775	45	82.45
100	VSS2	-454	-424.775	45	82.45

#	Pad Name	X	Y	W	H
101	VSS2	-394	-424.775	45	82.45
102	VSS2	-334	-424.775	45	82.45
103	VSS2	-274	-424.775	45	82.45
104	VSS2	-214	-424.775	45	82.45
105	VSS2	-154	-424.775	45	82.45
106	VSS2	-94	-424.775	45	82.45
107	VDD2	-34	-424.775	45	82.45
108	VDD2	26	-424.775	45	82.45
109	VDD2	86	-424.775	45	82.45
110	VDD2	146	-424.775	45	82.45
111	VDD2	206	-424.775	45	82.45
112	VDD2	266	-424.775	45	82.45
113	VDD2	326	-424.775	45	82.45
114	VDD2	386	-424.775	45	82.45
115	VDD2	446	-424.775	45	82.45
116	VDD2	506	-424.775	45	82.45
117	VDD2	566	-424.775	45	82.45
118	VDD2	626	-424.775	45	82.45
119	VDD2	686	-424.775	45	82.45
120	VDD2	746	-424.775	45	82.45
121	VDD3	806	-424.775	45	82.45
122	VDD3	866	-424.775	45	82.45
123	VDD3	926	-424.775	45	82.45
124	VDD3	986	-424.775	45	82.45
125	VDD3	1046	-424.775	45	82.45
126	VDD	1106	-424.775	45	82.45
127	VDD	1166	-424.775	45	82.45
128	VDD	1226	-424.775	45	82.45
129	VDD	1286	-424.775	45	82.45
130	VDD	1346	-424.775	45	82.45
131	VDD	1406	-424.775	45	82.45
132	VDD	1466	-424.775	45	82.45
133	VDD	1526	-424.775	45	82.45
134	VDD	1586	-424.775	45	82.45
135	VDD	1646	-424.775	45	82.45
136	VDD	1706	-424.775	45	82.45
137	VDD	1766	-424.775	45	82.45
138	VDD	1826	-424.775	45	82.45
139	VDD	1886	-424.775	45	82.45
140	TST2_pad	1946	-424.775	45	82.45
141	TST2_pad	2006	-424.775	45	82.45
142	TST4_pad	2095	-424.775	45	82.45
143	TST4_pad	2155	-424.775	45	82.45
144	TST4_pad	2215	-424.775	45	82.45
145	TST4_pad	2275	-424.775	45	82.45
146	TST4_pad	2335	-424.775	45	82.45
147	VLCDIN_pad	2395	-424.775	45	82.45
148	VLCDIN_pad	2455	-424.775	45	82.45
149	VLCDIN_pad	2515	-424.775	45	82.45
150	VLCDIN_pad	2575	-424.775	45	82.45
151	VLCDOUT_pad	2670.7	-424.775	45	82.45
152	VLCDOUT_pad	2730.7	-424.775	45	82.45

#	Pad Name	X	Y	W	H
153	VLCDOUT_pad	2790.7	-424.775	45	82.45
154	VLCDOUT_pad	2850.7	-424.775	45	82.45
155	VLCDOUT_pad	2910.7	-424.775	45	82.45
156	VA0N_pad	2970.7	-424.775	45	82.45
157	VA0N_pad	3030.7	-424.775	45	82.45
158	VA0N_pad	3090.7	-424.775	45	82.45
159	VA1N_pad	3170.7	-424.775	45	82.45
160	VA1N_pad	3230.7	-424.775	45	82.45
161	VA1N_pad	3290.7	-424.775	45	82.45
162	VA1P_pad	3370.7	-424.775	45	82.45
163	VA1P_pad	3430.7	-424.775	45	82.45
164	VA1P_pad	3490.7	-424.775	45	82.45
165	VA0P_pad	3570.7	-424.775	45	82.45
166	VA0P_pad	3630.7	-424.775	45	82.45
167	VA0P_pad	3690.7	-424.775	45	82.45
168	VB0N_pad	3770.7	-424.775	45	82.45
169	VB0N_pad	3830.7	-424.775	45	82.45
170	VB0N_pad	3890.7	-424.775	45	82.45
171	VB1N_pad	3970.7	-424.775	45	82.45
172	VB1N_pad	4030.7	-424.775	45	82.45
173	VB1N_pad	4090.7	-424.775	45	82.45
174	VB1P_pad	4182.3	-424.775	45	82.45
175	VB1P_pad	4242.3	-424.775	45	82.45
176	VB1P_pad	4302.3	-424.775	45	82.45
177	VB0P_pad	4382.5	-424.775	45	82.45
178	VB0P_pad	4442.5	-424.775	45	82.45
179	VB0P_pad	4502.5	-424.775	45	82.45
180	DUMMY3	4768.5	-458	135	15
181	COM<160>	4768.5	-431	135	15
182	COM<158>	4768.5	-404	135	15
183	COM<156>	4768.5	-377	135	15
184	COM<154>	4768.5	-350	135	15
185	COM<152>	4768.5	-323	135	15
186	COM<150>	4768.5	-296	135	15
187	COM<148>	4768.5	-269	135	15
188	COM<146>	4768.5	-242	135	15
189	COM<144>	4768.5	-215	135	15
190	COM<142>	4768.5	-188	135	15
191	COM<140>	4768.5	-161	135	15
192	COM<138>	4768.5	-134	135	15
193	COM<136>	4768.5	-107	135	15
194	COM<134>	4768.5	-80	135	15
195	COM<132>	4768.5	-53	135	15
196	COM<130>	4768.5	-26	135	15
197	COM<128>	4768.5	1	135	15
198	COM<126>	4768.5	28	135	15
199	COM<124>	4768.5	55	135	15
200	COM<122>	4768.5	82	135	15
201	COM<120>	4768.5	109	135	15
202	COM<118>	4768.5	136	135	15
203	COM<116>	4768.5	163	135	15
204	COM<114>	4768.5	190	135	15

#	Pad Name	X	Y	W	H
205	COM<112>	4768.5	217	135	15
206	COM<110>	4768.5	244	135	15
207	COM<108>	4768.5	271	135	15
208	COM<106>	4768.5	298	135	15
209	COM<104>	4768.5	325	135	15
210	COM<102>	4768.5	352	135	15
211	COM<100>	4768.5	379	135	15
212	COM<98>	4768.5	406	135	15
213	DUMMY4	4768.5	433	135	15
214	COM<96>	4576.5	418.5	15	135
215	COM<94>	4549.5	418.5	15	135
216	COM<92>	4522.5	418.5	15	135
217	COM<90>	4495.5	418.5	15	135
218	COM<88>	4468.5	418.5	15	135
219	COM<86>	4441.5	418.5	15	135
220	COM<84>	4414.5	418.5	15	135
221	COM<82>	4387.5	418.5	15	135
222	COM<80>	4360.5	418.5	15	135
223	COM<78>	4333.5	418.5	15	135
224	COM<76>	4306.5	418.5	15	135
225	COM<74>	4279.5	418.5	15	135
226	COM<72>	4252.5	418.5	15	135
227	COM<70>	4225.5	418.5	15	135
228	COM<68>	4198.5	418.5	15	135
229	COM<66>	4171.5	418.5	15	135
230	COM<64>	4144.5	418.5	15	135
231	COM<62>	4117.5	418.5	15	135
232	COM<60>	4090.5	418.5	15	135
233	COM<58>	4063.5	418.5	15	135
234	COM<56>	4036.5	418.5	15	135
235	COM<54>	4009.5	418.5	15	135
236	COM<52>	3982.5	418.5	15	135
237	COM<50>	3955.5	418.5	15	135
238	COM<48>	3928.5	418.5	15	135
239	COM<46>	3901.5	418.5	15	135
240	COM<44>	3874.5	418.5	15	135
241	COM<42>	3847.5	418.5	15	135
242	COM<40>	3820.5	418.5	15	135
243	COM<38>	3793.5	418.5	15	135
244	COM<36>	3766.5	418.5	15	135
245	COM<34>	3739.5	418.5	15	135
246	COM<32>	3712.5	418.5	15	135
247	COM<30>	3685.5	418.5	15	135
248	COM<28>	3658.5	418.5	15	135
249	COM<26>	3631.5	418.5	15	135
250	COM<24>	3604.5	418.5	15	135
251	COM<22>	3577.5	418.5	15	135
252	COM<20>	3550.5	418.5	15	135
253	COM<18>	3523.5	418.5	15	135
254	COM<16>	3496.5	418.5	15	135
255	COM<14>	3469.5	418.5	15	135
256	COM<12>	3442.5	418.5	15	135

#	Pad Name	X	Y	W	H
257	COM<10>	3415.5	418.5	15	135
258	COM<8>	3388.5	418.5	15	135
259	COM<6>	3361.5	418.5	15	135
260	COM<4>	3334.5	418.5	15	135
261	COM<2>	3307.5	418.5	15	135
262	SEG<1>	3226.5	418.5	15	135
263	SEG<2>	3199.5	418.5	15	135
264	SEG<3>	3172.5	418.5	15	135
265	SEG<4>	3145.5	418.5	15	135
266	SEG<5>	3118.5	418.5	15	135
267	SEG<6>	3091.5	418.5	15	135
268	SEG<7>	3064.5	418.5	15	135
269	SEG<8>	3037.5	418.5	15	135
270	SEG<9>	3010.5	418.5	15	135
271	SEG<10>	2983.5	418.5	15	135
272	SEG<11>	2956.5	418.5	15	135
273	SEG<12>	2929.5	418.5	15	135
274	SEG<13>	2902.5	418.5	15	135
275	SEG<14>	2875.5	418.5	15	135
276	SEG<15>	2848.5	418.5	15	135
277	SEG<16>	2821.5	418.5	15	135
278	SEG<17>	2794.5	418.5	15	135
279	SEG<18>	2767.5	418.5	15	135
280	SEG<19>	2740.5	418.5	15	135
281	SEG<20>	2713.5	418.5	15	135
282	SEG<21>	2686.5	418.5	15	135
283	SEG<22>	2659.5	418.5	15	135
284	SEG<23>	2632.5	418.5	15	135
285	SEG<24>	2605.5	418.5	15	135
286	SEG<25>	2578.5	418.5	15	135
287	SEG<26>	2551.5	418.5	15	135
288	SEG<27>	2524.5	418.5	15	135
289	SEG<28>	2497.5	418.5	15	135
290	SEG<29>	2470.5	418.5	15	135
291	SEG<30>	2443.5	418.5	15	135
292	SEG<31>	2416.5	418.5	15	135
293	SEG<32>	2389.5	418.5	15	135
294	SEG<33>	2362.5	418.5	15	135
295	SEG<34>	2335.5	418.5	15	135
296	SEG<35>	2308.5	418.5	15	135
297	SEG<36>	2281.5	418.5	15	135
298	SEG<37>	2254.5	418.5	15	135
299	SEG<38>	2227.5	418.5	15	135
300	SEG<39>	2200.5	418.5	15	135
301	SEG<40>	2173.5	418.5	15	135
302	SEG<41>	2146.5	418.5	15	135
303	SEG<42>	2119.5	418.5	15	135
304	SEG<43>	2092.5	418.5	15	135
305	SEG<44>	2065.5	418.5	15	135
306	SEG<45>	2038.5	418.5	15	135
307	SEG<46>	2011.5	418.5	15	135
308	SEG<47>	1984.5	418.5	15	135

#	Pad Name	X	Y	W	H
309	SEG<48>	1957.5	418.5	15	135
310	SEG<49>	1930.5	418.5	15	135
311	SEG<50>	1903.5	418.5	15	135
312	SEG<51>	1876.5	418.5	15	135
313	SEG<52>	1849.5	418.5	15	135
314	SEG<53>	1822.5	418.5	15	135
315	SEG<54>	1795.5	418.5	15	135
316	SEG<55>	1768.5	418.5	15	135
317	SEG<56>	1741.5	418.5	15	135
318	SEG<57>	1714.5	418.5	15	135
319	SEG<58>	1687.5	418.5	15	135
320	SEG<59>	1660.5	418.5	15	135
321	SEG<60>	1633.5	418.5	15	135
322	SEG<61>	1606.5	418.5	15	135
323	SEG<62>	1579.5	418.5	15	135
324	SEG<63>	1552.5	418.5	15	135
325	SEG<64>	1525.5	418.5	15	135
326	SEG<65>	1498.5	418.5	15	135
327	SEG<66>	1471.5	418.5	15	135
328	SEG<67>	1444.5	418.5	15	135
329	SEG<68>	1417.5	418.5	15	135
330	SEG<69>	1390.5	418.5	15	135
331	SEG<70>	1363.5	418.5	15	135
332	SEG<71>	1336.5	418.5	15	135
333	SEG<72>	1309.5	418.5	15	135
334	SEG<73>	1282.5	418.5	15	135
335	SEG<74>	1255.5	418.5	15	135
336	SEG<75>	1228.5	418.5	15	135
337	SEG<76>	1201.5	418.5	15	135
338	SEG<77>	1174.5	418.5	15	135
339	SEG<78>	1147.5	418.5	15	135
340	SEG<79>	1120.5	418.5	15	135
341	SEG<80>	1093.5	418.5	15	135
342	SEG<81>	1066.5	418.5	15	135
343	SEG<82>	1039.5	418.5	15	135
344	SEG<83>	1012.5	418.5	15	135
345	SEG<84>	985.5	418.5	15	135
346	SEG<85>	958.5	418.5	15	135
347	SEG<86>	931.5	418.5	15	135
348	SEG<87>	904.5	418.5	15	135
349	SEG<88>	877.5	418.5	15	135
350	SEG<89>	850.5	418.5	15	135
351	SEG<90>	823.5	418.5	15	135
352	SEG<91>	796.5	418.5	15	135
353	SEG<92>	769.5	418.5	15	135
354	SEG<93>	742.5	418.5	15	135
355	SEG<94>	715.5	418.5	15	135
356	SEG<95>	688.5	418.5	15	135
357	SEG<96>	661.5	418.5	15	135
358	SEG<97>	634.5	418.5	15	135
359	SEG<98>	607.5	418.5	15	135
360	SEG<99>	580.5	418.5	15	135

#	Pad Name	X	Y	W	H
361	SEG<100>	553.5	418.5	15	135
362	SEG<101>	526.5	418.5	15	135
363	SEG<102>	499.5	418.5	15	135
364	SEG<103>	472.5	418.5	15	135
365	SEG<104>	445.5	418.5	15	135
366	SEG<105>	418.5	418.5	15	135
367	SEG<106>	391.5	418.5	15	135
368	SEG<107>	364.5	418.5	15	135
369	SEG<108>	337.5	418.5	15	135
370	SEG<109>	310.5	418.5	15	135
371	SEG<110>	283.5	418.5	15	135
372	SEG<111>	256.5	418.5	15	135
373	SEG<112>	229.5	418.5	15	135
374	SEG<113>	202.5	418.5	15	135
375	SEG<114>	175.5	418.5	15	135
376	SEG<115>	148.5	418.5	15	135
377	SEG<116>	121.5	418.5	15	135
378	SEG<117>	94.5	418.5	15	135
379	SEG<118>	67.5	418.5	15	135
380	SEG<119>	40.5	418.5	15	135
381	SEG<120>	13.5	418.5	15	135
382	SEG<121>	-13.5	418.5	15	135
383	SEG<122>	-40.5	418.5	15	135
384	SEG<123>	-67.5	418.5	15	135
385	SEG<124>	-94.5	418.5	15	135
386	SEG<125>	-121.5	418.5	15	135
387	SEG<126>	-148.5	418.5	15	135
388	SEG<127>	-175.5	418.5	15	135
389	SEG<128>	-202.5	418.5	15	135
390	SEG<129>	-229.5	418.5	15	135
391	SEG<130>	-256.5	418.5	15	135
392	SEG<131>	-283.5	418.5	15	135
393	SEG<132>	-310.5	418.5	15	135
394	SEG<133>	-337.5	418.5	15	135
395	SEG<134>	-364.5	418.5	15	135
396	SEG<135>	-391.5	418.5	15	135
397	SEG<136>	-418.5	418.5	15	135
398	SEG<137>	-445.5	418.5	15	135
399	SEG<138>	-472.5	418.5	15	135
400	SEG<139>	-499.5	418.5	15	135
401	SEG<140>	-526.5	418.5	15	135
402	SEG<141>	-553.5	418.5	15	135
403	SEG<142>	-580.5	418.5	15	135
404	SEG<143>	-607.5	418.5	15	135
405	SEG<144>	-634.5	418.5	15	135
406	SEG<145>	-661.5	418.5	15	135
407	SEG<146>	-688.5	418.5	15	135
408	SEG<147>	-715.5	418.5	15	135
409	SEG<148>	-742.5	418.5	15	135
410	SEG<149>	-769.5	418.5	15	135
411	SEG<150>	-796.5	418.5	15	135
412	SEG<151>	-823.5	418.5	15	135

#	Pad Name	X	Y	W	H
413	SEG<152>	-850.5	418.5	15	135
414	SEG<153>	-877.5	418.5	15	135
415	SEG<154>	-904.5	418.5	15	135
416	SEG<155>	-931.5	418.5	15	135
417	SEG<156>	-958.5	418.5	15	135
418	SEG<157>	-985.5	418.5	15	135
419	SEG<158>	-1012.5	418.5	15	135
420	SEG<159>	-1039.5	418.5	15	135
421	SEG<160>	-1066.5	418.5	15	135
422	SEG<161>	-1093.5	418.5	15	135
423	SEG<162>	-1120.5	418.5	15	135
424	SEG<163>	-1147.5	418.5	15	135
425	SEG<164>	-1174.5	418.5	15	135
426	SEG<165>	-1201.5	418.5	15	135
427	SEG<166>	-1228.5	418.5	15	135
428	SEG<167>	-1255.5	418.5	15	135
429	SEG<168>	-1282.5	418.5	15	135
430	SEG<169>	-1309.5	418.5	15	135
431	SEG<170>	-1336.5	418.5	15	135
432	SEG<171>	-1363.5	418.5	15	135
433	SEG<172>	-1390.5	418.5	15	135
434	SEG<173>	-1417.5	418.5	15	135
435	SEG<174>	-1444.5	418.5	15	135
436	SEG<175>	-1471.5	418.5	15	135
437	SEG<176>	-1498.5	418.5	15	135
438	SEG<177>	-1525.5	418.5	15	135
439	SEG<178>	-1552.5	418.5	15	135
440	SEG<179>	-1579.5	418.5	15	135
441	SEG<180>	-1606.5	418.5	15	135
442	SEG<181>	-1633.5	418.5	15	135
443	SEG<182>	-1660.5	418.5	15	135
444	SEG<183>	-1687.5	418.5	15	135
445	SEG<184>	-1714.5	418.5	15	135
446	SEG<185>	-1741.5	418.5	15	135
447	SEG<186>	-1768.5	418.5	15	135
448	SEG<187>	-1795.5	418.5	15	135
449	SEG<188>	-1822.5	418.5	15	135
450	SEG<189>	-1849.5	418.5	15	135
451	SEG<190>	-1876.5	418.5	15	135
452	SEG<191>	-1903.5	418.5	15	135
453	SEG<192>	-1930.5	418.5	15	135
454	SEG<193>	-1957.5	418.5	15	135
455	SEG<194>	-1984.5	418.5	15	135
456	SEG<195>	-2011.5	418.5	15	135
457	SEG<196>	-2038.5	418.5	15	135
458	SEG<197>	-2065.5	418.5	15	135
459	SEG<198>	-2092.5	418.5	15	135
460	SEG<199>	-2119.5	418.5	15	135
461	SEG<200>	-2146.5	418.5	15	135
462	SEG<201>	-2173.5	418.5	15	135
463	SEG<202>	-2200.5	418.5	15	135
464	SEG<203>	-2227.5	418.5	15	135

#	Pad Name	X	Y	W	H
465	SEG<204>	-2254.5	418.5	15	135
466	SEG<205>	-2281.5	418.5	15	135
467	SEG<206>	-2308.5	418.5	15	135
468	SEG<207>	-2335.5	418.5	15	135
469	SEG<208>	-2362.5	418.5	15	135
470	SEG<209>	-2389.5	418.5	15	135
471	SEG<210>	-2416.5	418.5	15	135
472	SEG<211>	-2443.5	418.5	15	135
473	SEG<212>	-2470.5	418.5	15	135
474	SEG<213>	-2497.5	418.5	15	135
475	SEG<214>	-2524.5	418.5	15	135
476	SEG<215>	-2551.5	418.5	15	135
477	SEG<216>	-2578.5	418.5	15	135
478	SEG<217>	-2605.5	418.5	15	135
479	SEG<218>	-2632.5	418.5	15	135
480	SEG<219>	-2659.5	418.5	15	135
481	SEG<220>	-2686.5	418.5	15	135
482	SEG<221>	-2713.5	418.5	15	135
483	SEG<222>	-2740.5	418.5	15	135
484	SEG<223>	-2767.5	418.5	15	135
485	SEG<224>	-2794.5	418.5	15	135
486	SEG<225>	-2821.5	418.5	15	135
487	SEG<226>	-2848.5	418.5	15	135
488	SEG<227>	-2875.5	418.5	15	135
489	SEG<228>	-2902.5	418.5	15	135
490	SEG<229>	-2929.5	418.5	15	135
491	SEG<230>	-2956.5	418.5	15	135
492	SEG<231>	-2983.5	418.5	15	135
493	SEG<232>	-3010.5	418.5	15	135
494	SEG<233>	-3037.5	418.5	15	135
495	SEG<234>	-3064.5	418.5	15	135
496	SEG<235>	-3091.5	418.5	15	135
497	SEG<236>	-3118.5	418.5	15	135
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499	SEG<238>	-3172.5	418.5	15	135
500	SEG<239>	-3199.5	418.5	15	135
501	SEG<240>	-3226.5	418.5	15	135
502	COM<1>	-3307.5	418.5	15	135
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505	COM<7>	-3388.5	418.5	15	135
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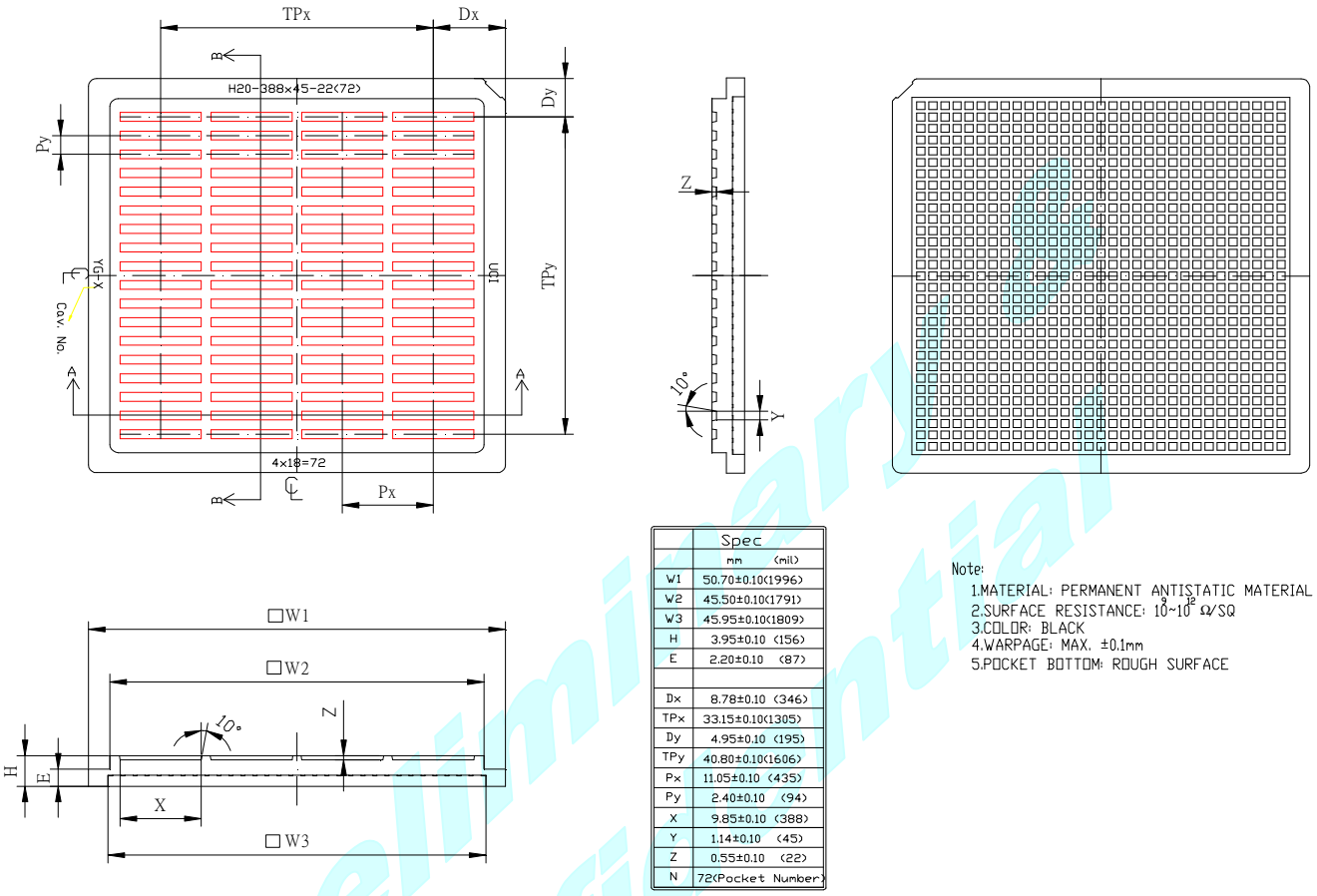
507	COM<11>	-3442.5	418.5	15	135
508	COM<13>	-3469.5	418.5	15	135
509	COM<15>	-3496.5	418.5	15	135
510	COM<17>	-3523.5	418.5	15	135
511	COM<19>	-3550.5	418.5	15	135
512	COM<21>	-3577.5	418.5	15	135
513	COM<23>	-3604.5	418.5	15	135
514	COM<25>	-3631.5	418.5	15	135
515	COM<27>	-3658.5	418.5	15	135
516	COM<29>	-3685.5	418.5	15	135

#	Pad Name	X	Y	W	H
517	COM<31>	-3712.5	418.5	15	135
518	COM<33>	-3739.5	418.5	15	135
519	COM<35>	-3766.5	418.5	15	135
520	COM<37>	-3793.5	418.5	15	135
521	COM<39>	-3820.5	418.5	15	135
522	COM<41>	-3847.5	418.5	15	135
523	COM<43>	-3874.5	418.5	15	135
524	COM<45>	-3901.5	418.5	15	135
525	COM<47>	-3928.5	418.5	15	135
526	COM<49>	-3955.5	418.5	15	135
527	COM<51>	-3982.5	418.5	15	135
528	COM<53>	-4009.5	418.5	15	135
529	COM<55>	-4036.5	418.5	15	135
530	COM<57>	-4063.5	418.5	15	135
531	COM<59>	-4090.5	418.5	15	135
532	COM<61>	-4117.5	418.5	15	135
533	COM<63>	-4144.5	418.5	15	135
534	COM<65>	-4171.5	418.5	15	135
535	COM<67>	-4198.5	418.5	15	135
536	COM<69>	-4225.5	418.5	15	135
537	COM<71>	-4252.5	418.5	15	135
538	COM<73>	-4279.5	418.5	15	135
539	COM<75>	-4306.5	418.5	15	135
540	COM<77>	-4333.5	418.5	15	135
541	COM<79>	-4360.5	418.5	15	135
542	COM<81>	-4387.5	418.5	15	135
543	COM<83>	-4414.5	418.5	15	135
544	COM<85>	-4441.5	418.5	15	135
545	COM<87>	-4468.5	418.5	15	135
546	COM<89>	-4495.5	418.5	15	135
547	COM<91>	-4522.5	418.5	15	135
548	COM<93>	-4549.5	418.5	15	135
549	COM<95>	-4576.5	418.5	15	135

TRAY INFORMATION



	Spec mm (mil)
W1	50.70±0.10(1996)
W2	45.50±0.10(1791)
W3	45.95±0.10(1809)
H	3.95±0.10 (156)
E	2.20±0.10 (87)
Dx	8.78±0.10 (346)
TPx	33.15±0.10(1305)
Dy	4.95±0.10 (195)
TPy	40.80±0.10(1606)
Px	11.05±0.10 (435)
Py	2.40±0.10 (94)
X	9.85±0.10 (388)
Y	1.14±0.10 (45)
Z	0.55±0.10 (22)
N	72(Pocket Number)

Note:
1.MATERIAL: PERMANENT ANTISTATIC MATERIAL
2.SURFACE RESISTANCE: 10^{9}~10^{12} Ω/SQ
3.COLOR: BLACK
4.WARPAGE: MAX. ±0.1mm
5.POCKET BOTTOM: ROUGH SURFACE

REVISION HISTORY

Revision	Contents	Date
	N/A	